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Phase-Cut Dimming for Solid State Lighting: Basic Compatibility

National Electrical Manufacturers Association

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Phase-Cut Dimming for Solid State Lighting: Basic Compatibility

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Foreword

The NEMA Solid State Lighting section has prepared this standard, *Phase-Cut Dimming for Solid State Lighting: Basic Compatibility*. This standard provides compatibility requirements for phase-cut dimming for LED light engines and is suitable for global use.

In the preparation of this standard, input of users and other interested parties has been sought and evaluated. Inquiries, comments, and proposed or recommended revisions should be submitted to the concerned NEMA product subdivision by contacting:

Senior Technical Director, Operations
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Section approval of the standard does not necessarily imply that all section members voted for its approval or participated in its development.

At the time the standard was approved, the Lighting Controls and Light Source sections were composed of the following members:

Acuity Brands Lighting
Advanced Lighting Technologies
Cree, Inc.
Eaton Lighting Solutions
EiKO, Ltd.
Enerlites Inc.
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Schneider Electric
Southwire Company
Technical Consumer Products, Inc.

Universal Lighting Technologies
Ushio America, Inc.
WattStopper
Westinghouse Lighting

CONTENTS

FIGURES

TABLES

Section 1
GENERAL

1.1 Scope

This standard provides compatibility requirements when a forward phase-cut dimmer is combined with one or more dimmable LED Light Engines (LLEs). An LLE, for the purposes of this document, comprises one or more LED modules, LED control gear (integral or remote), and a connection to the mains circuit[1]. Three configurations of LED light engines are shown below (Figure 1-1).

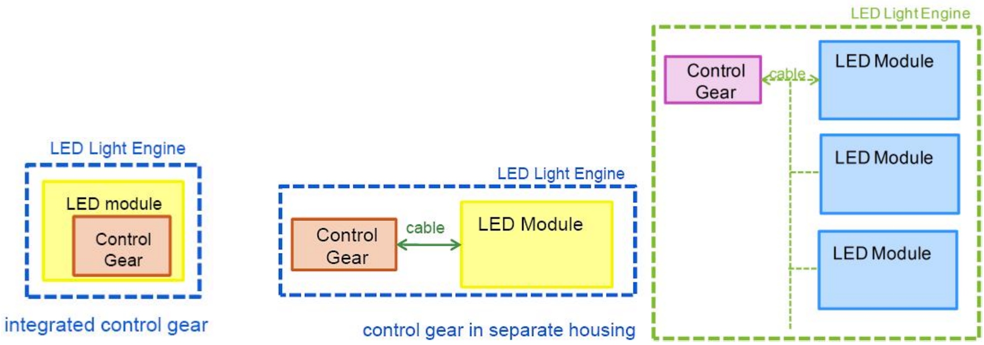

Figure 1-1
LED Light Engine

The requirements in this standard do not limit its use to any specific lighting product type or application, and it is suitable for use globally. For the purposes of this standard, *compatibility* means:

a. The reliability of the dimmer and LLE are not affected by combining them.
b. Dimming behavior meets or exceeds the behavior specified in sections 3 and 4.

Any interfaces between control gear and LED module(s) within the LLE are undefined in this standard. Such an interface may take a variety of forms. For example, it may be a constant voltage interface, a constant current interface, or a low-voltage alternating current interface produced by control gear that is simply a step-down electronic transformer. In all cases, compatibility is only defined for the LLE (which may contain one or more specific combinations of control gear and LED module(s)), and not for either component independently. To be considered compliant with this standard, the control gear and modules shall be operated together. This standard does not preclude future standards that will permit separate qualification of control gear and module components, with interfaces defined between them that ensure a proper SSL 7A LLE interface from the point of view of this standard.

This standard is forward-looking and is intended to be used to design and qualify dimmer and LLE products (including integral or remote control gear) for use with each other. It is not intended for use to determine compatibility with existing products or the installed base of LLEs and phase-cut dimmers. For information on compatibility with the installed base of dimmers, see SSL 6-2010.

NOTE—Any requirement for compliance to this standard does not supersede applicable international or local regulation.

[1] Through an ANSI/IEC base or a non-ANSI/IEC interface.

1.1 Organization

This standard is organized in two parts. Part A covers the minimum requirements for compatibility. Part B covers minimum requirements for performance. This document describes only Part A. SSL 7B is currently under development.

The standard is predicated on being able to separate the dimmer and LLE for independent testing. Synthetic loads (representing an LLE) are defined for testing of dimmers, and waveform generators (representing a dimmer) are defined for testing of LLEs. As a result of this separation, the specifications and testing are separated into a dimmer and an LLE section. Proper performance of the LLE with the waveform generators ensures that the LLE will meet the compatibility requirements with dimmers that have been designed using the synthetic loads. Similarly, proper performance of the dimmer with the synthetic loads ensures compatibility when operating with an LLE that has been designed using the waveform generators.

Many tests included in this specification may be application dependent. Therefore, a manufacturer should consider the need to conduct the tests for various installation applications.

1.2 Normative References

The following normative documents contain provisions which, through reference in this text, constitute provisions of this standards publication. By reference herein these publications are adopted, in whole or in part as indicated, in this standards publication.

ANSI/IES RP-16-10	*Nomenclature and Definitions for Illuminating Engineering*
IEC 60038 Ed. 7.0	*IEC Standard Voltages*
IEC 60669-2-1 Ed 4.1 2009-01	*Switches for Household and Similar Fixed-Electrical Installations– Part 2-1: Particular Requirements–Electronic Switches*
NEMA 410-2011	*Performance Testing for Lighting Controls and Switching Devices with Electronic Drivers and Discharge Ballasts*

1.3 Informative References

ISO/IEC 17025: 2005	*General requirements for the competence of testing and calibration laboratories*
NEMA PB 1-2011	*Panelboards*
NEMA SSL 6-2010	*Solid State Lighting for Incandescent Replacement Dimming,* with April 2011 Errata

1.4 Definitions

compatible: Two components of a system, for example a dimmer and a light source, when combined, provide basic functionality as described in SSL 7A. For the purposes of this standard, compatibility means: 1) the reliability of the dimmer and LLE are not affected by combining them and 2) dimming behavior meets or exceeds the behavior specified in sections 3 and 4.

conduction angle: In the case of a forward phase dimmer, conduction angle is the phase angle (180-0 degrees) measured from the point where conduction begins (for the purposes of this standard, conduction is defined as when the voltage across the load exceeds 20% of instantaneous line voltage at that point) to the next zero cross location (beginning of the next half-cycle). See Figure 2-1.

phase-cut dimmer: A dimmer, for the purposes of this standard, is a control unit that produces a forward phase (leading edge) ac waveform. This dimmer output waveform is supplied to one or more LLEs. The conduction angle of the waveform is adjustable. (See Figure 2-1 for an example of a forward phase dimmer output waveform.)

electronic control gear (ECG): Electronic control gear is the electronics that converts ac mains into a signal that drives the LEDs (or LED module). The electronic control gear may be integrated into an LLE or it may be a separate module that drives an LED module. Also known as a *driver*.

inrush current: Waveform of the input current, measured immediately after the input voltage is connected.

interchangeable: Two components of one type (for example dimmers) are interchangeable if they are both compatible with a component of another type (for example, a light source) and operate with comparable performance. For example, the dimmers have the same dimming curve.

interoperable: See *Compatible*.

LED light engine or lamp (LLE): A combination of one electronic control gear and one or more LED modules. The gear and LED modules may or may not be integrated into a single unit.

NOTE—This standard uses LLE to include *LED Light Engine* as defined by IES (RP-16) and *LED Lamp* as defined by IES (RP-16). An LLE may or may not have a base.

minimum dimmer load: The dimmer manufacturer's specified operating limit in watts or number of LLEs, below which proper operation of the dimmer is not assured.

maximum light output (MLO): Light output (luminous flux) produced by a LLE when connected directly on nominal mains voltage without a dimmer. See Figure 4-1.

nominal mains voltage: Nominal mains voltage is defined by IEC 60038.

off-state (dimmer): When the dimmer is producing electrical signals below a phase angle specified in section 3.8 intended to put the LLE in the off-state.

off-state (LLE): When the LLE is producing less than 0.05% of the maximum light output or 2 lumens (whichever is more), the LLE is considered to be in the off-state.

on-state (dimmer): When the dimmer is producing electrical signals intended to put the LLE in the on-state.

on-state (LLE): When the LLE is producing more than or equal to the minimum light output, the LLE is considered in the on-state.

rated wattage (LLE): Rated wattage is the manufacturer specified power, in watts, drawn by the LLE when it is connected directly to the nominal mains voltage without a dimmer. For practical purposes, rated Wattage is calculated as Vrms * Irms * PF. Rated Wattage may be rounded up to the next whole number.

rated wattage (dimmer): The manufacturer specified maximum sum of rated wattages of LLEs that can be connected to the dimmer without causing damage, taking into consideration maximum continuous current, maximum inrush current, maximum repetitive peak current, and maximum RMS current when the LLE is dimmed.

reference minimum light output (RMLO): The light output (luminous flux) produced by a LLE when connected to a phase-cut dimmer set to produce a conduction angle specified in section 4.8.2. See Figure 4-1.

repetitive peak current: The periodic peak input current, measured during steady state. This peak occurs in each half cycle of the mains.

repetitive peak ring-up voltage: This is a damped oscillatory wave superimposed on the mains whose amplitude after reaching a maximum decreases gradually with time. This periodic phenomenon (corresponding to each of the dimmer's commutations) is the result of the energy restored by the reactive components, forming a resonant circuit, in the dimmer and/or in the LLE (coil and capacitor).

Section 2
BACKGROUND

2.1 Phase-Control Dimming

Two types of phase-control dimmers exist: forward phase and reverse phase. Forward phase-control dimmers (sometimes also called leading-edge dimmers or simply, but somewhat inaccurately, incandescent dimmers) vary a load's brightness by changing the amount of delay from a zero crossing in the sine wave until the time they begin conducting current to the load. Light output increases as conduction angle increases. For some phase-control dimmers, it is not possible for the conduction angle to extend completely to the zero-crossing.

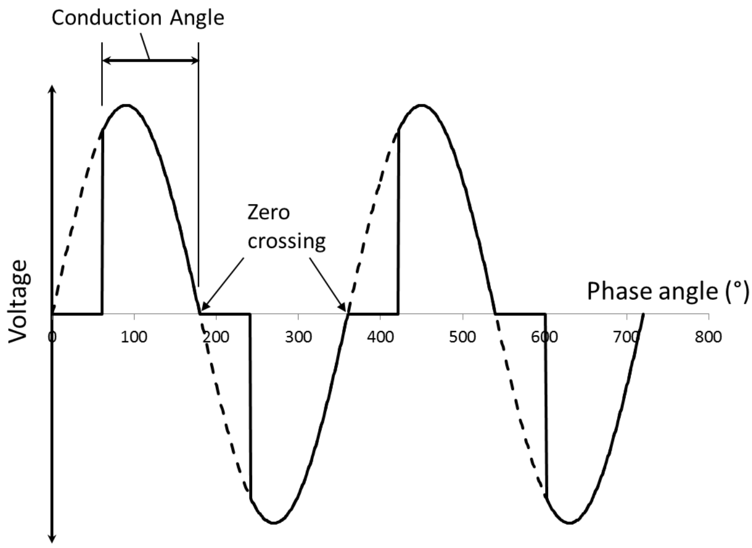

Figure 2-1
Generic Waveform Produced By A Forward Phase-Control (Leading Edge) Dimmer

Forward phase-control dimmers have a design that can be created with a variety of power semiconductors, including thyristors or transistors.

Note that some controls may be designed to be universal dimmers, supporting either forward or reverse phase operation in the same device. The actual mode of operation is selected through automatic detection or manual configuration means.

This document specifies compability requirements for the use of forward phase dimmers with LLEs.

2.2 LLE/Dimmer Compatibility Factors

The important factors that influence LLE/dimmer compatibility include:

a. The dimming method (forward phase cut for SSL 7A compliance)
b. Inrush current (to both dimmer and LLE)
c. Repetitive peak current (to both dimmer and LLE)

d. Rated power (of both LLE and dimmer)
e. Repetitive peak ring-up voltage (at LLE/dimmer interface)
f. Minimum light output (LLE)
g. Maximum RMS current.
h. Minimum conduction angle (dimmer)
i. Maximum light output (LLE)
j. Maximum conduction angle (dimmer)
k. Off-state dimmer supply current
l. On-state dimmer supply current
m. LLE impedance in various operating modes
n. Ability of the dimmer to synchronize by detecting mains zero crossing through the LLE

These factors are addressed in the specifications in sections 3 through 5.

Section 3
DIMMER

3.1 General

This section describes the specifications and testing procedures for forward phase-cut dimmers to ensure compatibility with dimmable LLEs. The testing described in this section is to be done with the synthetic load (Figure A-1 and Figure A-2) described in Annex A.2-A.3 at all rated mains voltages.

SSL 7A-compliant dimmers may be capable of multiple operation modes through manual configuration means. However, they are compliant only when set to a SSL 7A-compliant mode.

The dimmer manufacturer is responsible for ensuring the reliability (lifetime) of the dimmer with respect to the tests included in section 3. This standard specifies the synthetic load used for such testing. If the dimmer manufacturer specifies a minimum or maximum load as a number of LLEs, then the following tests shall be performed with the appropriate number of synthetic loads matching that specified number of LLEs.

3.2 Rated Wattage

The rated wattage is not determined by this standard, but rather assigned by the manufacturer. This rated wattage shall be used to determine values for the tests in sections 3.3 through 3.9.

3.3 Forward Phase-Control Stability Requirements

The dimmer shall generate a stable output waveform, as measured on the synthetic load shown in Annex A.2 and Annex A.3, which has a rising edge (voltage goes from near-zero to near-line voltage) that changes as the user changes the control's input. Stable operation means that with no changes to control input (steady-state), no two half-cycle conduction angles shall vary by more than 10 degrees (this represents ±5 degrees) from each other over 10 full line cycles.

The phase-control stability testing is conducted with the dimmer connected to the synthetic load shown in the specified annex. The test is conducted at the following conditions:

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a. The dimmer is connected to the synthetic load circuits as described below. The load is set to represent the dimmer's *minimum* dimmer load. For dimmers with no minimum dimmer load, 5W shall be used. Stable operation shall be confirmed at maximum and minimum conduction angles, as described above.
   1. The test shall be conducted with the low power factor synthetic load shown in Annex A.2.
   2. The test shall be repeated with the high power factor synthetic load shown in Annex A.3.

b. The dimmer is connected to the synthetic load circuits as described below. The load is set to represent the dimmer's rated wattage. Stable operation shall be confirmed at maximum and minimum conduction angles, as described above.
   1. The test shall be conducted with the low power factor synthetic load shown in Annex A.2.
   2. The test shall be repeated with the high power factor synthetic load shown in Annex A.3.

3.4 Inrush Current

Inrush current is caused by initially applying power to the LLE. This current can stress mechanical switch and semiconductor components inside the dimmer and shall be limited.

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The dimmer manufacturer shall ensure that the dimmer is rated for the inrush current when operated with the synthetic load in Annex A.2 per the dimmer's rated wattage (section 3.2) by testing at the following conditions:

a. The dimmer is set to its maximum conduction angle.
b. The dimmer is set to 90 degree conduction angle.

To ensure compliance with this test, repeat 10 times. The recorded value shall be the maximum of the 10 trials.

Some dimmers may have *soft-start* capabilities, which means they automatically start at a small conduction angle when turned on, and fade to a higher level. For testing dimmers with this functionality, the fade-on time shall be set to its minimum time (if adjustable). The test shall then be performed with the dimmer set to reach the desired conduction angle (specified above) at the end of the fade.

3.5 Repetitive Peak Current

Electronic control gear used in LLEs may generate repetitive peak current. This can cause stress on semiconductor components inside the dimmer.

The dimmer manufacturer shall ensure that the dimmer can handle the worst case repetitive peak current of the LLE when operated with the synthetic load in Annex A.2 with values selected using the rated wattage of the dimmer (section 3.2) from Table A-2 to A-5, depending on the mains voltage. The test shall be conducted with the dimmer set to 90 degrees conduction angle. The dimmer is run until reaching steady state and the manufacturer shall ensure that all components are operating within their design specifications.

3.6 Overload

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While overload is not a normal operation, the dimmer manufacturer shall ensure the dimmer can withstand overloaded operation when operated with the synthetic load in Annex A.2 and values selected using 120% of the rated wattage of the dimmer (section 3.2) by testing at the following conditions:

a. The dimmer is set to its maximum conduction angle and allowed to reach steady state.
b. The dimmer is set to a 90 degree conduction angle and allowed to reach steady state.

At the conclusion of the overload tests, a dimmer shall still be able to perform its intended function, although lifetime may be impacted by the test. The dimmer is run until reaching steady state and the manufacturer shall ensure that all components are operating within their design specifications.

3.7 Repetitive Peak Voltage

The repetitive peak voltage testing is conducted with the dimmer connected to a fixed resistive load representing the minimum dimmer load or 5W, whichever is greater. A dimmer shall not produce a repetitive peak voltage across the load higher than 145% of peak of the applied mains (Table 1). The test is conducted at the following condition:

a. The dimmer is placed at 90 degree conduction angle.

NOTE—Testing of dimmers with LLEs and incandescents have shown that the repetitive peak voltage observed with an LLE is less than that of an incandescent at 230VAC, and within 8% of that of an incandescent at 120VAC. Worst case repetitive peak voltage occurs with a 90 degree conduction angle and with a single LLE. Although repetitive peak voltage does not appear to be a major impediment to compatibility, it may affect LLE or dimmer reliability, therefore, a specification based on incandescent behavior is defined below.

Table 3-1
Repetitive Peak Voltage Limit Table (Dimmer)

Voltage	Ring Up Limit
100V	210V
120V	250V
230V	480V
277V	570V

Determined by V_{MAINS_RMS} * sqrt(2) * 1.45 and then rounded up to the next ten.

3.8 Minimum On-State Conduction Angle

The minimum stable light output of the LLE occurs at a conduction angle that allows enough energy to be present to operate the electronics in the LLE. A dimmer shall output a phase-cut waveform with a conduction angle of 40 degrees ±5 degrees, when set to its minimum dimmed level. A dimmer which has an adjustable minimum setting is SSL 7A-compliant only when its minimum setting is adjusted within the minimum on-state conduction range shown in Figure 4-1. When in the on-state, the dimmer shall not output a conduction angle of less than 35 degrees when in an SSL 7A-compliant state.

The test for this section shall be performed twice using the figure in Annex A.3 with component values selected to produce a wattage equal to:

a. Rated dimmer wattage
b. Minimum dimmer load. For dimmers with no minimum rating, 5W shall be used.

3.9 Maximum On-State Conduction Angle

The dimmer shall output a conduction angle greater than or equal to 130 degrees when set to produce maximum light level in the on-state. A dimmer which has an adjustable maximum setting is SSL 7A-compliant only when its maximum setting satisfies this minimum conduction angle.

The test for this section shall be done in conjunction with the circuit in Annex A.3 with component values selected to produce a wattage equal to:

a. Rated dimmer wattage
b. Minimum dimmer load. For dimmers with no minimum rating, 5W shall be used.

3.10 Off-State Operation

3.10.1 Background

Many dimmers with advanced features require current to be passed through the load in the off-state, in order to allow a proper path for their internal power supply to charge (in the absence of a neutral wire, which is uncommon in typical installations). The dimmer power supply operates over a wide range of unknown load impedances. Within that range, the dimmer limits its peak current to minimize power dissipation. The intent of this test is to make sure the peak currents required by the dimmer fall within a defined range over a variety of LLE impedances.

3.10.2 Test

The dimmer shall be tested in accordance with Figure 3-1 with switch S1 closed. The dimmer is set to its off-state, and resistor R1 is initially set to the maximum value of the X-axis of Figure 3-2 or Figure 3-3 (depending on mains voltage). The dimmer shall function properly in the off-state as determined by the manufacturer, including taking into account the minimum number of LLEs as defined by the manufacturer. (To simulate a load representing multiple LLEs, a second resistor may be connected in parallel with R1, and its value shall be adjusted to match the value of R1 during testing.) The peak current through R1 is measured. The measured peak current shall fall below the limits set forth below. The resistance is swept to the minimum value of the X-axis using those values shown in Figure 3-2 or Figure 3-3. Over all resistance values, the peak current shall not exceed the limits as shown in Figures 3-2 and 3-3, and the dimmer shall continue to function properly as determined by the manufacturer.

Additionally, dimmers shall also satisfy the following test:

a. Set the impedance to the minimum value of the X-axis in Figure 3-2 or Figure 3-3.
b. Verify that the dimmer continues to operate properly, including taking into account the minimum number of LLEs as defined by the manufacturer.
c. Open the switch S1. The dimmer shall continue to operate for 0.5 seconds.

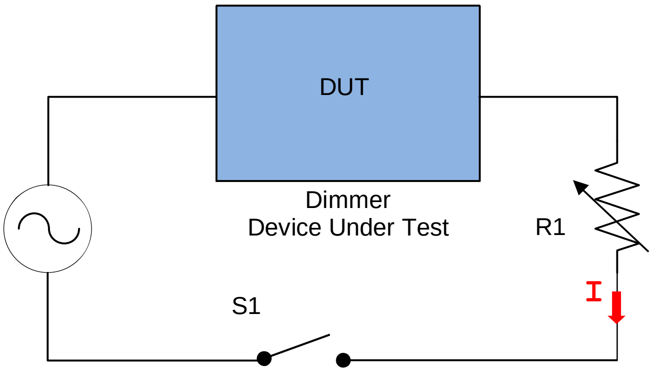

Figure 3-1
Circuit For Off-State Testing Of Dimmers

NOTE—For mains supply, use line characteristics given in Table A-1.

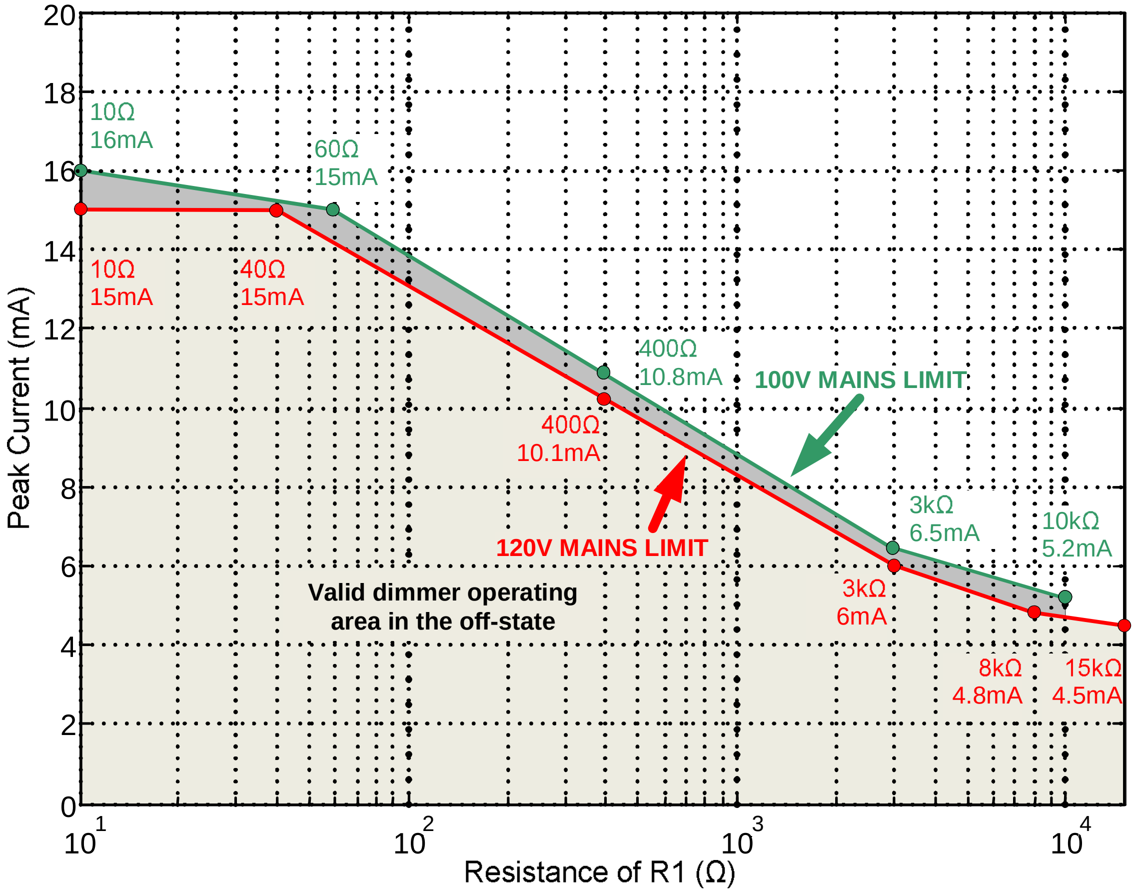

Figure 3-2
Dimmer Allowable Off-State Current
(100V and 120V MAINS)

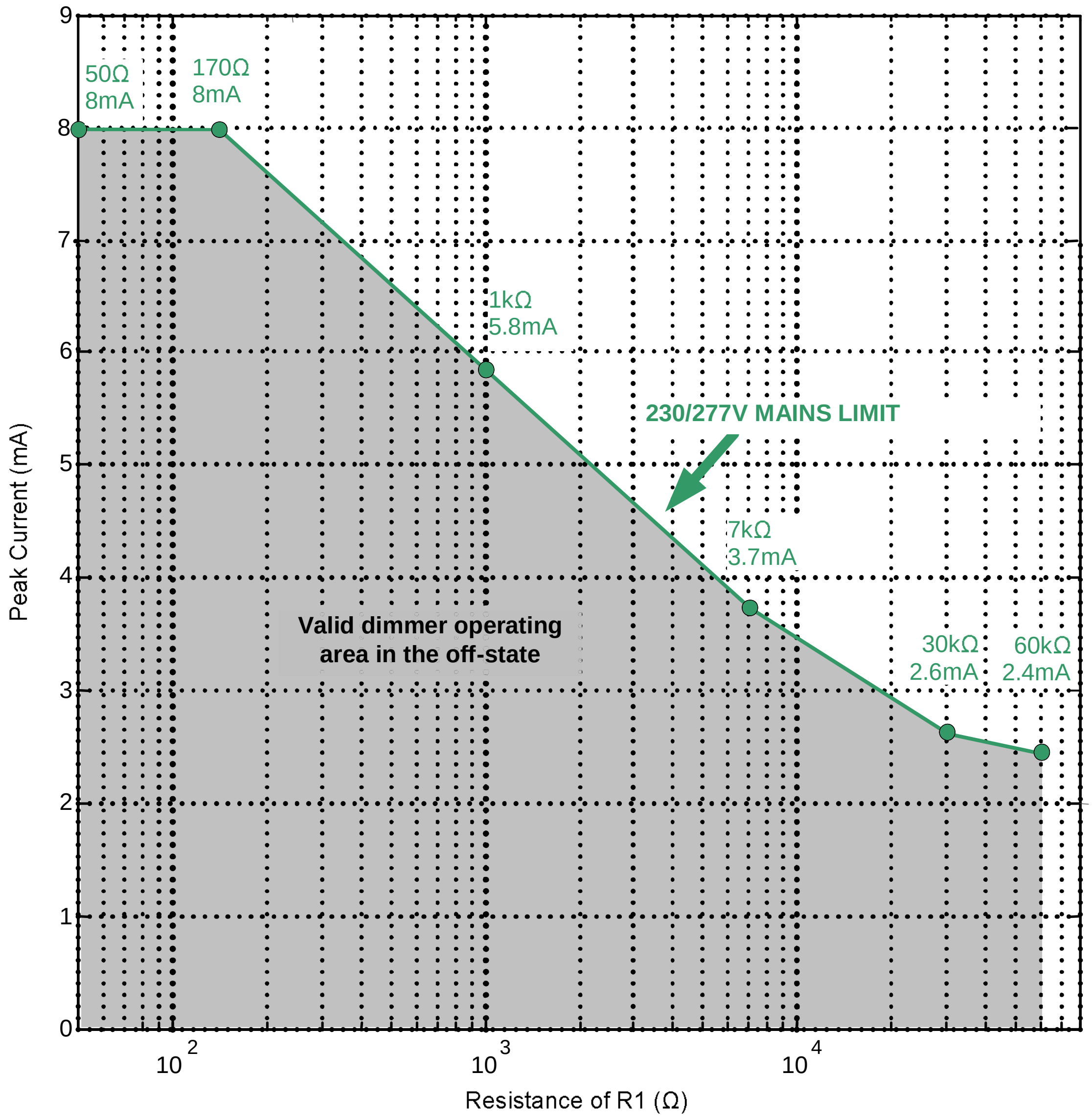

Figure 3-3
Dimmer Allowable Off-State Current
(230V and 277V MAINS)

3.11 On-State Dimmer Supply Current

The dimmer shall be connected per Figure A-2 in Annex A.3 set to the minimum load as defined by the dimmer manufacturer. Voltage shall be measured across the dimmer DUT and current shall be measured through R_{on}, as shown in the schematic.

The resistance value for R_{on} shall be set to the rightmost point shown in Figure 3-4 or Figure 3-5 (depending on mains voltage). With the dimmer DUT replaced by a shunt, the value of R2 is adjusted until the peak current is equal to the value of the rightmost point of Figure 3-4 or 3-5.

The shunt is replaced by the dimmer DUT, and the dimmer manufacturer shall confirm that the dimmer DUT is functioning properly across the range of conduction angles and that its maximum conduction angle is not less than 130 degrees, including taking into account the minimum number of LLEs as defined by the manufacturer. This process is to be repeated with the remaining highlighted points in Figure 3-4 or 3-5 (the points may be tested in any order). (To simulate a load representing multiple LLEs, a second circuit from Figure A-2 in Annex A.3 may be connected in parallel with the first one, and its shall be independently adjusted in the manner described above during testing.)

NOTE—It is expected that the amplitude of the dimmer on-state current decreases when the conduction angle is reduced, as power required is approximately constant regardless of conduction angle.

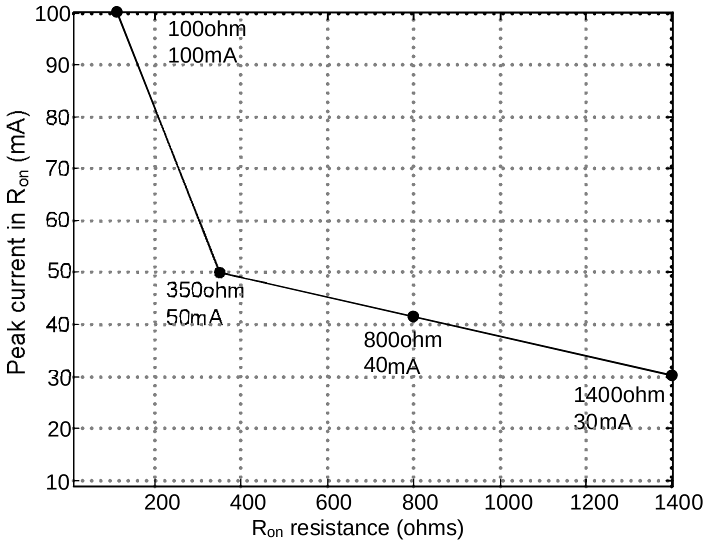

Figure 3-4
Dimmer Allowable On-State Dimmer Supply Current
(100V and 120V MAINS)

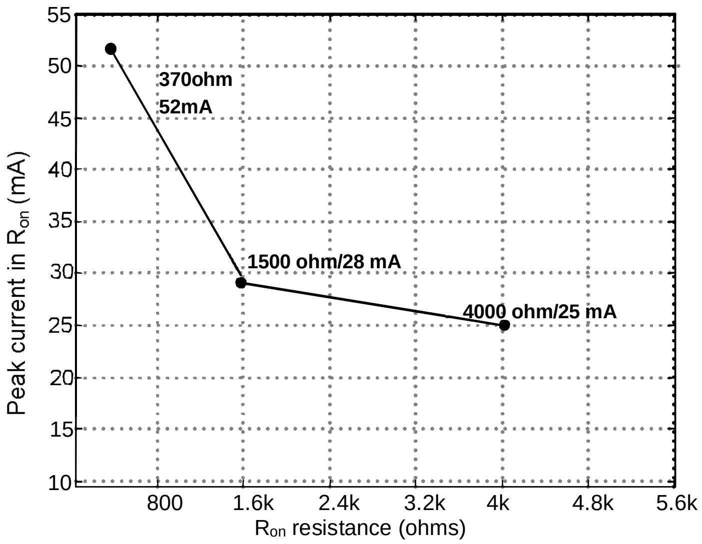

Figure 3-5
Dimmer Allowable On-State Dimmer Supply Current
(230V and 277V MAINS)

3.12 Marking Requirements

3.12.1 Maximum Rated Wattage

A dimmer shall be permanently marked with its maximum rated wattage. The rated wattage shall be provided to the nearest watt.

3.12.2 Minimum Load

If the dimmer requires a minimum load for proper operation (such as described in Section 3.10.2 or 3.11), the product packaging shall declare the minimum load value in watts or number of SSL 7A-compliant LLEs. No minimum load marking means that the minimum load is 5W (or less), or 1 SSL 7A-compliant LLE.

3.12.3 Operating Voltage

The nominal mains voltage(s) at which the dimmer is designed to operate shall be marked on the dimmer.

3.12.4 Dimmers with Multiple Modes

A dimmer may offer multiple modes of operation, not all of which are SSL 7A-compliant. Product instructions shall provide information on how to put product in SSL 7A-compliant mode, when multiple modes are available. *Universal dimmers* with only automatic load type detection must default to SSL 7A-compliant mode and shall not change mode when tested with the synthetic loads defined in this document.

Section 4
LLE

This section describes the specifications and testing procedures for LLEs to ensure compatibility with compliant dimmers. The testing described in this section is to be done with the waveform generators described in Annex A.4 and A.5, applied to the LLE.

4.1 Phase-Control Requirements

LLEs shall be capable of being dimmed with a forward phase-cut waveform per section 2.1.

A LLE may support being dimmed with a reverse phase-cut waveform but that performance is not considered in this standard. All testing in this section shall be performed with a forward phase waveform.

4.2 Rated Wattage

During dimmed operation, the power consumed by the LLE shall be no more than 110% of the power measured without a dimmer at rated line voltage or an increase of 2W, whichever is greater.

4.3 Power Factor

LLEs shall have a power factor ≥ 0.5 when operated on nominal mains voltage without a dimmer.

4.4 Maximum RMS Current

The maximum RMS current of a LLE during dimming shall be less than 200% of the RMS current that the LLE draws when connected to specified mains voltage without a dimmer.

The LLE manufacturer shall check for compliance by completing the following procedure using the waveform generator in Figure A-4.

a. Measure the LLE's nominal RMS current while operating on mains voltage without a dimmer.
b. Set the waveform generator at the maximum conduction angle and slowly reduce the conduction angle to the minimum value while measuring the current of the LLE. Record the maximum measured RMS current.

At no time shall the measured RMS current exceed 200% of the nominal RMS current as determined in step 1.

4.5 Inrush Current

The LLE limit shall be tested using the test circuit shown in Annex A.4 for this specified section.

To test an LLE or control gear:

1. Connect device under test to terminals of the circuit in Figure A-3 or equivalent circuit.
2. Connect current probe between L1 and DUT.
3. Turn on mains voltage and allow 10 seconds or more to charge.
4. Close S1 and measure the current amplitude.
5. Remove Mains voltage and reverse polarity of DUT.
6. Repeat test from steps 2-4. Inrush current value is the maximum of the two measured values.

The amplitude of the inrush current drawn by the LLE test load shall not exceed the rated wattage of the LLE test load multiplied by the inrush peak current ratios as defined in Table 4-1. The ratios depend (nonlinearly) on the power consumed by the LLE load. Depending on the power consumed by a single LLE, sufficient LLEs may be combined to make a load less than or equal to 10W, or a load less than or equal to 100W.

The amplitude of the I^2t drawn by the LLE test load shall not exceed the rated wattage of the LLE test load multiplied by the I^2t ratios (Table 4-1). The ratios depend (nonlinearly) on the power consumed by the LLE load. Depending on the power consumed by a single LLE, sufficient LLEs shall be combined to make a load less than or equal to 10W, or a load less than or equal to 100W.

NOTE—I^2t is calculated as $0.5 * I_{pk}^2 * t$ where I_{pk} = peak current and t = time from I_{pk} to $0.368* I_{pk}$.

NOTE—When measuring the inrush current of self-ballasted lamps, prior to the occurrence of I_{peak}, one or more current spikes may be observed which exceed the subsequent I_{peak} which are caused by EMI capacitors in the LLE. These spikes typically have durations of a few tens of microseconds, where the actual inrush current has a duration of, approximately, a few 100 microseconds. Such spike(s) do not significantly contribute to the inrush current and can be neglected by use of a digital filter with 50 microsecond window or low pass filter with 50 microsecond time constant or equivalent means. Only currents greater than 10% of I_{peak} shall be included in the inrush energy integral.

Table 4-1[2]
LLE Inrush Current Limits

Multiply per-Watt entries by the actual power connected.

Nominal Mains Voltage (V_{AC})	**Frequency (Hz)**	**Maximum Mains Impedance**		**Maximum Bulk Energy Capacitance (µF/A)**	**≤100W Load**			**≤10W Load**		
		Inductance (µH)	**Resistance (mΩ)**		**Maximum Inrush Peak Current Ratio (A/W)**	**Maximum Inrush I^2T (A^2s/W)**	**Maximum Repetitive Peak Current Ratio (A/W)**	**Maximum Inrush Peak Current Ratio (A/W)**	**Maximum Inrush I^2T (A^2s/W)**	**Maximum Repetitive Peak Current Ratio (A/W)**
100	50	400	200	175	0.7825	0.01621	0.111	1.649	0.003125	0.2587
100	60	400	200	175	0.7804	0.01589	0.0988	1.65	0.00309	0.218
120	60	100	450	175	1.0296	0.01903	0.128	2.006	0.00414	0.2329
230	50	400	200	125	0.8797	0.01252	0.07725	1.45	0.00206	0.1432
277	60	100	450	125	1.137	0.01561	0.087	1.629	0.00256	0.1193

4.6 Repetitive Peak Current

a. For LLEs with rated wattage less than or equal to 5W, the amplitude of the repetitive peak current shall not exceed 1A.
b. For LLEs with rated wattage greater than 5W, the amplitude of the repetitive peak current drawn by the LLE test load shall not exceed the rated wattage multiplied by the repetitive peak current ratio (Table 4-1). The ratios depend (nonlinearly) on the power consumed by the LLE load. Depending on the power consumed by a single LLE, sufficient LLEs may be combined to make a load less than or equal to 10W, or a load less than or equal to 100W.
c. The LLE repetitive peak current shall be tested using the test circuit shown in Annex A.5, with switch S2 closed and switch S3 open. Allow the circuit to stabilize for at least one second after

[2] Values in Table 4-1 were calculated by the method outlined in Annex A-1. Columns 1-5 are the input values used in the calculations.

applying mains voltage. Adjust the conduction angle via R4 to 90 degrees and measure the repetitive peak current through the LLE.

NOTE—When measuring the inrush current of self-ballasted lamps, prior to the occurrence of I_{peak}, one or more current spikes may be observed which exceed the subsequent I_{peak} which are caused by EMI capacitors in the LLE. These spikes typically have durations of a few tens of microseconds, where the actual inrush current has a duration of, approximately, a few 100 microseconds. Such spike(s) do not significantly contribute to the inrush current and can be neglected by use of a digital filter with 50 microsecond window or low pass filter with 50 microsecond time constant or equivalent means

The LLE manufacturer shall ensure reliability (lifetime) of the LLE under the defined repetitive peak current test conditions provided in Annex A.5.

4.7 Repetitive Peak Voltage

Repetitive peak voltage can affect compatibility in that the LLE can damage the dimmer and vice versa during stable operation. Research has shown that the worst case repetitive peak voltage occurs with a 90 degree conduction angle and with a single LLE.

The LLE shall be tested with the waveform generator in Annex A.5 at a conduction angle of 90 degrees with switch S2 closed and switch S3 open and per the requirements in Table 4-2. For the LLE to pass, the peak ring up voltage measured across the synthetic waveform generator (hot to dimmed hot),shall be less than the limits specified in Table 4-2.

Table 4-2
Repetitive Peak Voltage Table (LLE)

Mains Voltage	Ring Up Limit
100V	210V
120V	250V
230V	480V
277V	570V

Determined by V_{MAINS_RMS} * sqrt(2) * 1.45 and then rounded up to the next ten.

4.8 Light Output

4.8.1 Maximum Light Output on a Dimmer

The maximum dimmed light output of the LLE shall be measured as follows:

1) Connect the LLE to the circuit in Annex A.5 with switch S2 closed and switch S3 open. Apply mains voltage and allow the circuit to stabilize for at least one second. Vary over the entire range of attainable conduction angles by adjusting R4 (see note in Annex A.5). The light output of the LLE shall be measured by a method consistent with IES LM-79. Record the conduction angle at which the maximum dimmed light output occurs.
2) The measured maximum dimmed light output shall occur when the conduction angle is above 130 degrees.
3) For the attainable conduction angles between 130 degrees and 180 degrees, LLE light output shall not exceed the MLO by more than 10% or fall below the MLO by more than 25% (upper right rectangle in Figure 4-1.)

4.8.2 Minimum Light Output on a Dimmer

The minimum dimmed light output of the LLE shall be measured as follows:

a. Connect the LLE to the circuit in Annex A.5 with switch S2 closed and switch S3 open. Apply mains voltage and allow the circuit to stabilize for at least one second. Vary over the range of conduction angles 35 to 130 degrees. The light output of the LLE shall be measured by a method consistent with IES LM-79. Record the conduction angle at which the minimum dimmed light output occurs.
b. The measured minimum dimmed light output shall occur when the conduction angle is between 45 degrees and 35 degrees. The LLEs shall be providing some visible light at 45 degrees.

The RMLO of the LLE is measured at a conduction angle of 40 degrees and shall not be more than 30% of the MLO. If the LLE is in the off-state at 40 degrees then the RMLO shall be measured at 45 degrees.

LLE light output below a conduction angle of 35 degrees is not relevant for operation on SSL7A compliant dimmers.

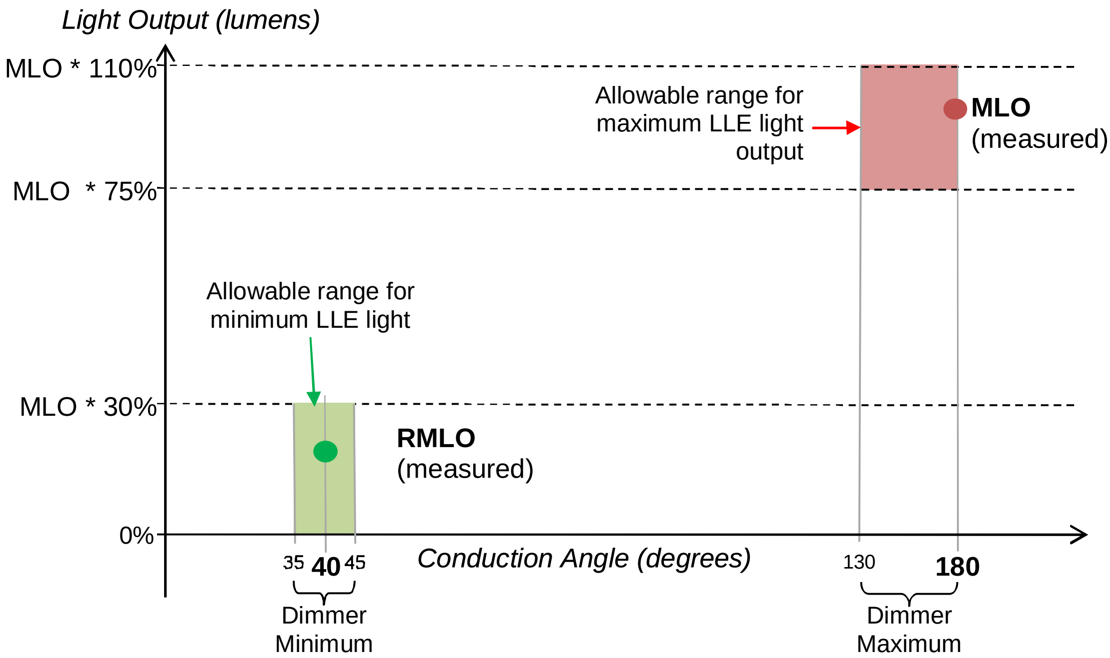

Figure 4-1
Light Output

4.9 Off-State Operation

4.9.1 Background

Dimmers and sensors that have no access to the neutral conductor may need to pass current through the load, *when the LLE is in the off-state*, in order to provide standby power to the dimmer and enable the dimmer functions. Examples include:

1) Dimmers that have an internal microprocessor that remains powered (e.g. to maintain pre-set levels/times),
2) dimmers that have a display that remains active,
3) dimmers that have an integrated nightlight, and

4) dimmer/LLE systems that include an occupancy sensor that requires power during the off-state.

If the load is unable to supply the current required by the dimmer or sensor during the off-state, then the dimmer and sensor are not likely to function properly.

The purpose of this section is to describe the ability of the SSL 7A-compliant LLE to pass current when the LLE is in the off-state. Section 3.10 describes the current that the SSL 7A-compliant dimmer may require from the load.

4.9.2 Testing

The LLE shall be connected to the synthetic waveform generator shown in Figure A-4 in Annex A.5. Switch S2 shall be set in the open position, setting the circuit in the *off-state*. Switch S3 shall be set in the closed position to enable the constant power circuit. Circuit values shall be chosen per Table A-9. Power is applied and the circuit is allowed to reach steady state. The instantaneous voltage across capacitor C5 shall be measured and shall not fall below values specified in Table 4-3 over the course of 10 seconds. As determined by the manufacturer, multiple identical LLEs may be connected in parallel to perform the testing (representing a minimum compliant load of more than one LLE).

Table 4-3
Limits for Off-State Operation Test

Mains Voltage	Minimum Voltage Across Capacitor C5 (V)
100	0.97
120	1.10
230	0.87
277	0.87

4.10 On-State Operation

4.10.1 Background

Two-wire dimmers require an allowable range of impedances (traditionally, resistive) in order to allow proper determination of conduction angle timing in relation to the zero cross. Since two-wire dimmers do not have neutral wires, and therefore do not have a direct reference between hot and neutral, the zero cross is detected through the impedance of the LLE. Additionally, the LLE has a defined impedance range which allows advanced-function dimmers (described previously) to properly charge their power supplies. The dimmer gets power for its internal power supply during the time when the switching device inside the dimmer (triac, FET, etc.) is not conducting.

4.10.2 Testing

The LLE shall be connected to the synthetic waveform generator shown in Figure A-4 in Annex A.5. Switch S2 shall be set in the closed position, setting the circuit in the on-state (phase-control signal generated). Switch S3 shall be set in the closed position to enable the constant power circuit. Circuit values shall be chosen per Table A-9. The synthetic waveform generator is set to a maximum conduction angle of 130 degrees via R4 (this represents the worst case, as the dimmer has the minimum amount of time to charge its internal supply). Superimpose the line voltage on phase-cut waveform to determine the exact location of zero cross, as distortion of the zero cross phase-cut waveform is possible. Power is applied and the circuit is allowed to reach steady state. The instantaneous voltage across capacitor C5 shall be measured and shall not fall below the values specified in Table 4-3 over the course of 10 seconds. As determined by the manufacturer, multiple identical LLEs may be connected in parallel to perform the testing (representing a minimum compliant load of more than one LLE).

4.11 Marking Requirements

4.11.1 RMLO

The RMLO shall be declared on the packaging as a percentage of maximum light output.

4.11.2 Minimum Load

If multiple LLEs are required for SSL-7A compliance (for example, as described in Section 4.9.2 and 4.10.2), then the LLE packaging shall be marked to indicate the minimum number of LLEs to pass SSL-7A tests. No marked minimum load indicates that only one LLE is requried.

ANNEX A
CIRCUITS (NORMATIVE)

A.1 Line Characteristics and Circuit Values

Relevant parameters and values used to determine the component values in the synthetic load are defined as follows. The formulas are provided for guidance, but the values may need to be adjusted to obtain the requirements of the synthetic load.

P_{avr} = RATED POWER of the dimmer (W)
f_{line} = line frequency (Hz)
V_{rms} = line rms voltage (Vrms)
PF = power factor at full conduction (dimensionless), assumed to be 0.5 for this test.
I_{rms} = current drawn by load at full conduction (Arms)
$I_{rms} = P_{avr} / (V_{rms}*PF)$
$1/x = f_{line}*R_{load}*C_{load}$ (dimensionless), assumed to be 4.5 for 60 Hz 120 Vac, assumed to be 7.8 for 60 Hz 277 Vac, *values for other frequencies and line voltages to be determined.*

The component values in the synthetic load circuit are determined as follows.
$R_{load} = 2*V_{rms}^2/P_{avr} * (1-e^{-x})/x$
$C_{load} = I_{rms} /(f_{line}*V_{rms}) * (PF/2)/(1-e^{-x})$
R_{esr1} and C_{load} are related by $R_{esr1} *C_{load}$ = 9 Ohms*22uF, for a typical electrolytic capacitor

Table A-1
Line Characteristics

Voltage	Resistance (mΩ)	Inductance (µH)	Reference Standard
100	200	400	No known reference standard. Values used in this document for 100V were assumed to be the IEC limits.
120	450	100	NEMA 410
230	200	400	IEC 60669 (Mains impedance is under consideration by IEC SC23B.)
277	450	100	NEMA 410

The values shown in the Tables A-2, A-3 A-4 and A-5 are approximate only. They shall be adjusted based on the input line characteristics of the test laboratory to achieve the values listed in the tables for all tests (inrush current, repetitive peak current, etc.).

Table A-2[3]
Synthetic Load Component Values (100V, 50/60HZ)

Simulated Power (W)	R_{load} (Ω)	C_{load} (μf)	R_{ESR1} of C_{load} (Ω max)	C_{rfi} (μF)	R_{on} (Ω)
5	3400	17.5	11.3	0.005	1.1k
50	340	175	1.13	0.05	
100	170	350	0.57	0.1	
150	113	525	0.38	0.15	
200	85	700	0.28	0.2	
250	68	875	0.23	0.25	
300	57	1050	0.19	0.3	
400	42.5	1400	0.14	0.4	
500	34	1750	0.11	0.5	
600	28	2100	0.094	0.6	
1000	17	3500	0.057	1	
1500	11	5250	0.038	1.5	
2000	8.5	7000	0.028	2	
2400	7	8400	0.024	2.4	

Table A-3[4]
Synthetic Load Component Values (120V, 60HZ)

Simulated Power (W)	R_{load} (Ω)	C_{load} (μf)	R_{ESR1} of C_{load} (Ω max)	C_{rfi} (μF)	R_{on} (Ω)
5	5200	14.5	14	0.005	1.4k
50	520	145	1.4	0.05	
100	260	290	0.68	0.1	
150	170	440	0.45	0.15	
200	130	580	0.34	0.2	
250	100	730	0.27	0.25	
300	86	870	0.23	0.3	
400	65	1160	0.17	0.4	
500	52	1450	0.14	0.5	
600	43	1740	0.12	0.6	
1000	26	2900	0.070	1.0	
1500	17	4350	0.045	1.5	
2000	13	5800	0.035	2.0	
2400	10	7000	0.028	2.4	

[3] Formulas may not match table values exactly due to rounding.
[4] Formulas may not match table values exactly due to rounding.

Table A-4[5]
Synthetic Load Component Values (230V, 50 HZ)

Simulated Power (W)	R_{load} (Ω)	C_{load} (µf)	R_{ESR1} of C_{load} (Ω max)	C_{rfi} (µF)	R_{on} (Ω)
5	19500	6.2	32	0.005	4.0k
50	1950	62	3.2	0.05	
100	975	124	1.6	0.1	
150	650	185	1.1	0.15	
200	490	250	0.80	0.2	
250	390	300	0.65	0.25	
300	325	370	0.57	0.3	
400	245	490	0.40	0.4	
500	195	620	0.32	0.5	
600	160	740	0.27	0.6	
1000	100	1250	0.16	1.0	
1500	65	1850	0.11	1.5	
2000	50	2450	0.080	2.0	
2400	40	3000	0.067	2.4	

[5] Formulas may not match table values exactly due to rounding.

Table A-5[6]
Synthetic Load Component Values (277V, 60HZ)

Simulated Power (W)	R_{load} (Ω)	C_{load} (µf)	R_{ESR1} of C_{load} (Ω max)	C_{rfi} (µF)	R_{on} (Ω)
5	29000	4.5	44	0.005	4.0k
50	2900	45	4.4	0.05	
100	1450	90	2.2	0.1	
150	960	135	1.5	0.15	
200	720	180	1.1	0.2	
250	575	225	0.88	0.25	
300	480	270	0.73	0.3	
400	360	360	0.55	0.4	
500	290	450	0.44	0.5	
600	240	540	0.37	0.6	
1000	145	900	0.22	1.0	
1500	96	1350	0.15	1.5	
2000	72	1800	0.11	2.0	
2400	60	2200	0.091	2.4	
3000	48	2700	0.073	3.0	
3500	41	3150	0.063	3.5	
4000	36	3600	0.055	4.0	
4500	32	4050	0.048	4.5	

The power supply used to test devices according this standard shall be in conformance with the power quality requirements described in the IECEE's CTL Operational Procedure, *Procedure for Measuring Laboratory Power Source Characteristics* (CTL-OP, 2007). (For example, in North America (Canada, US and Mexico), this is defined in NEMA PB 1-2011 *Panelboards*.) This is a current requirement for ISO/IEC 17025 *General Requirements for the Competence of Testing and Calibration Laboratories* approved laboratories globally.

[6] Formulas may not match table values exactly due to rounding.

A.2 Circuit 1 (Synthetic Load 1 for Dimmer Forward-Phase Stability, Inrush Current, Repetitive Peak Current and Overload Testing)

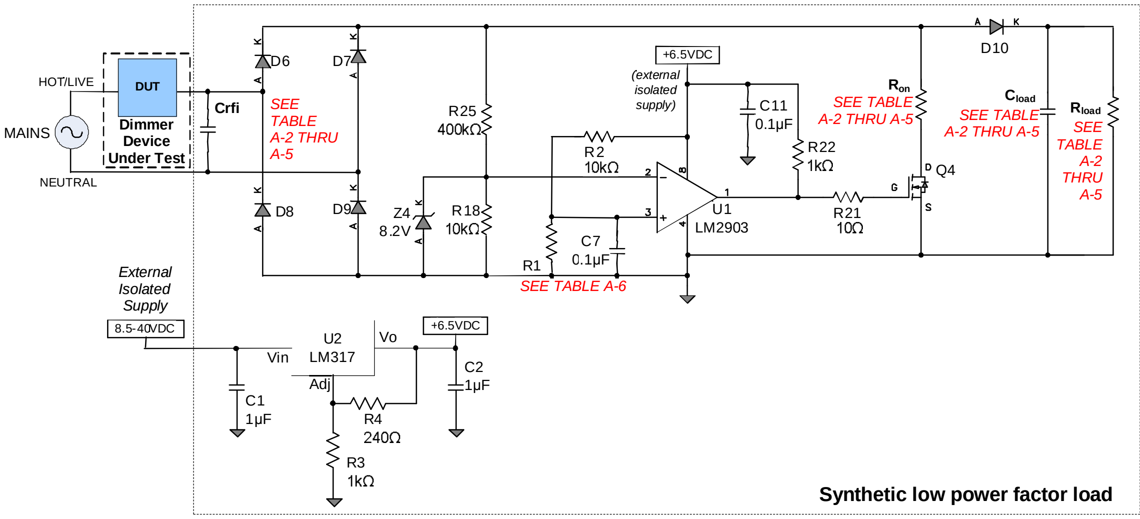

Figure A-1[7]
Circuit for Forward-Phase Stability, Inrush Current, Repetitive Peak Current and Overload Testing

This circuit represents a low power factor supply, with a *bleeder* resistor (R_{on}) added to maintain operation of a power supply that may be needed in a t-wire *smart dimmer*.

The RFI capacitor is added to more realistically simulate real-life LLEs, because large values of capacitance can cause stability problems with many common non-SSL 7A-compliant dimmers.

NOTE—This represents worst case capacitors that are commonly used in LLEs, it does not imply that RFI capacitors are required in the LLE.

The components are used to selectively insert R_{on} when the line voltage is below a threshold level, as determined by R1 and R2. R_{on} is intended to ensure that the power supply of the dimmer has a low-impedance path to operate, if needed. Values should be selected from Table A-6 based on the mains voltage of the LLE being simulated.

Table A-6
Component Values For Use in the Synthetic Load of Figure A-1

LLE simulated Voltage (V)	Frequency (Hz)	R1 (Ω)
100	60	2.94k
120	60	3.57k
230	50	11k
277	60	15k

Values of C_{rfi}, R_{on}, C_{load}, and R_{load} are found in Tables A-2 through A-4 depending on the applicable mains voltage.

[7] Schematics for synthetic circuits and waveform generators show typical components. Established electrical equivalents may be used.

A.3 Circuit 2 (Synthetic Load 2 for Dimmer for Forward-Phase Stability, Maximum and Minimum On-State Conduction Angle and On-State Operation Testing)

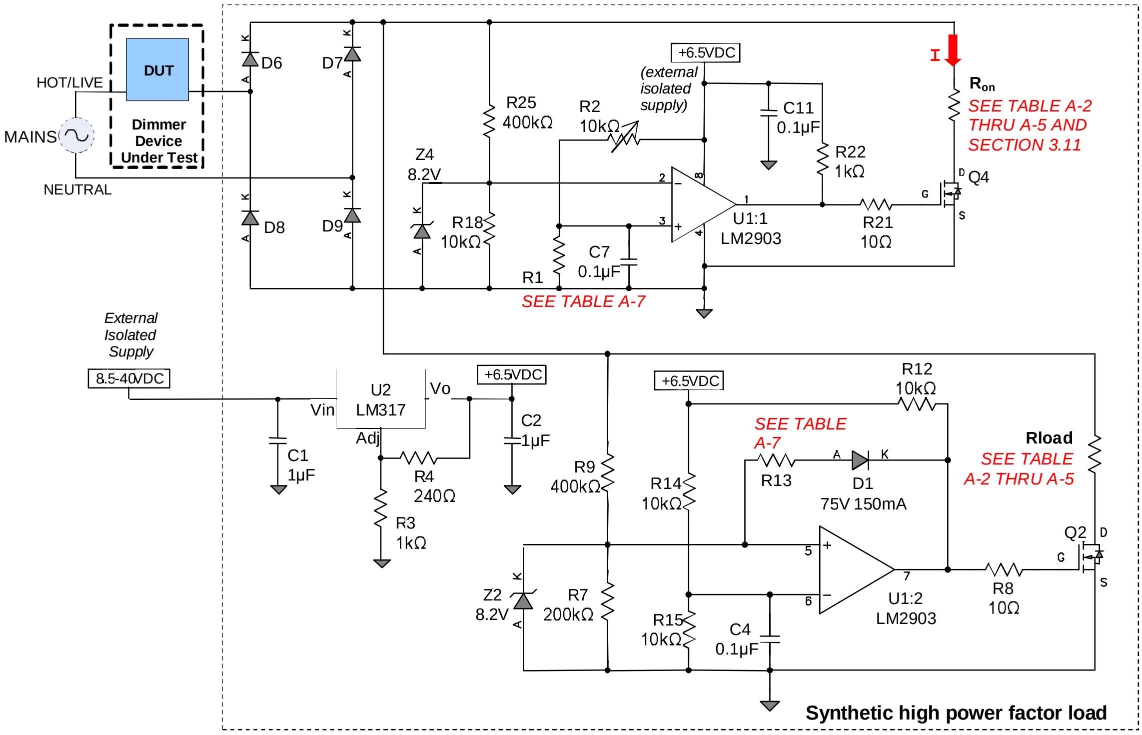

Figure A-2[8]
Circuit for Forward Phase Stability, Maximum and Minimum On-State Conduction Angle and On-State Operation Testing

This circuit represents a high power factor LLE. This circuit tests the ability of the control to operate on a load which looks nearly resistive. The RFI capacitor is removed to eliminate its leakage path. The circuit for R_{on} is the same as in the previous diagram. C_{load}, representing a very low power-factor load has been removed. Instead, the addition of the separate circuit in the dotted box adds a resistive load (R_{load}) when the line voltage is above a particular threshold, as determined by R1 and R2. This would represent the load in the operating state when the dimmer is conducting. This represents a worst case load for dimmers in that it only allows them to charge in the beginning of the half-cycle.

Values should be selected from Table A-7 based on the mains voltage of the LLE being simulated.

[8] Schematics for synthetic circuits and waveform generators show typical components. Established electrical equivalents may be used.

Table A-7
Component Values for Use in the Synthetic Load of Figure A-2

LLE simulated Voltage (V)	Frequency (Hz)	R13 (Ω)	R1 (Ω)
100	60	20.5k	2.94k
120	60	17k	3.57k
230	50	7.87k	11k
277	60	6.8k	15k

Values for R_{load} and R_{on} should be taken from Tables A-2 through A-5 depending on the mains voltage.

A.4 Circuit 3 (Waveform Generator for Inrush Current)

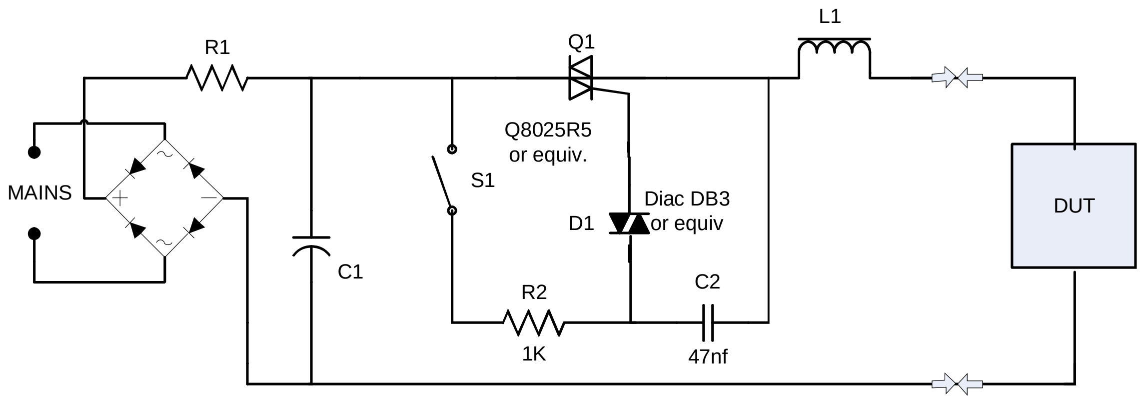

Figure A-3[9]
Waveform Generator for Inrush Test Current

NOTE—See Table A-8 for component values for Figure A-3.

Table A-8
Component Values for Use in the Waveform Generator of Figure A-3

C1	> 100µf and > 4 X total input capacitance value of DUT
R1	$< \frac{1\text{ second}}{C1}$ Note full charging time between tests > 10sec
L1	Inductor to match typical mains line characteristics, see Table A1.

[9] Schematics for synthetic circuits and waveform generators show typical components. Established electrical equivalents may be used.

A.5 Circuit 4 (Waveform Generator for Maximum RMS Current, Repetitive Peak Current, Repetitive Peak Voltage, Light Output, Off-State Operation, On-State Operation)

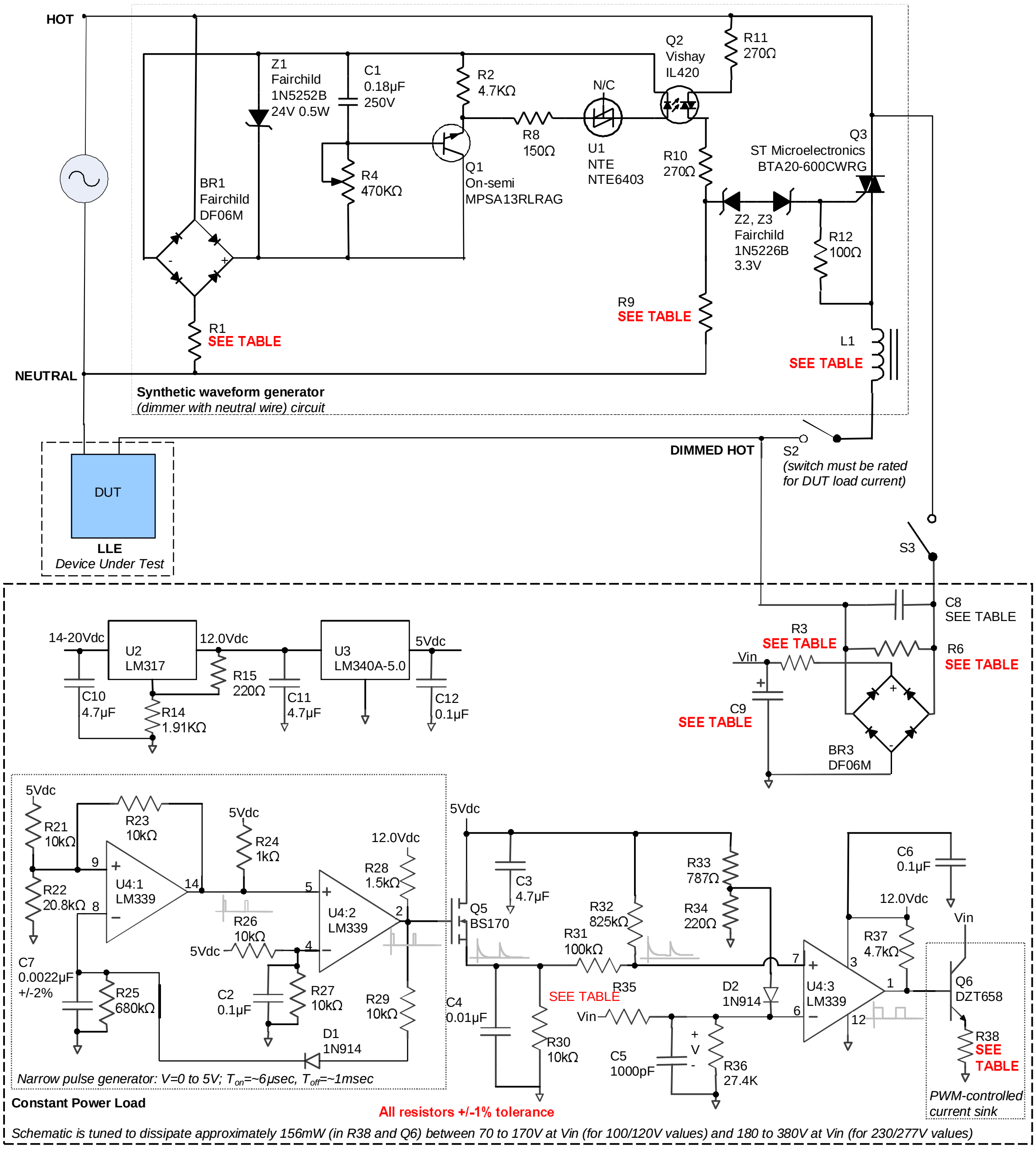

Figure A-4[10]
Waveform Generator for Maximum RMS Current, Repetitive Peak Current, Repetitive Peak Voltage, Light Output, Off-State Operation, On-State Operation

[10] Schematics for synthetic circuits and waveform generators show typical components. Established electrical equivalents may be used.

NOTE—For mains supply, use line characteristics given in Table A-1. Component R4 and C1 may need to modified to reach full maximum and minimum conduction angles at all test voltages and frequencies.

Table A-9
Waveform Generator Component Values

Mains Voltage	100 VAC 50/60 Hz	120 VAC 60 Hz	230 VAC 50 Hz	277 VAC 60 Hz	Comment
L1 (for 50-600W loads)	1mH @ 1kHz ±15% DCR < 0.5Ω	0.1mH @ 1kHz ±15% DCR <0.18Ω	1.3mH @ 1kHz ±15% DCR < 0.5Ω	0.1mH @ 1kHz ±15% DCR < 0.18Ω	L1 shall not saturate under entire connected nominal load range
R1 (kΩ)	33		66		2W rated
R9 (kΩ)	75		150		1W rated
R35 (MΩ)	2.2		5.1		
R38 (kΩ)	1.37		3.32		
R6 (kΩ)	500		1000		½W rated
R3 (Ω)	150		600		
C8 (μF)	0.01		0.0047		
C9 (μF)	10		3.3		

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