

具有成本效益的 bq297xx 电压和电流保护集成电路（适用于单节锂离子/锂聚合物电池）

1 特性

- 输入电压范围 Pack+: VSS - 0.3V 至 12V
- FET 驱动:
 - CHG 和 DSG FET 驱动输出
- 外部 FET 上针对过流保护 (OCP) 的电流感应在 $\pm 5\text{mV}$ (典型值) 以内
- 故障检测
 - 过度充电检测 (OVP)
 - 过度放电检测 (UVP)
 - 充电过流检测 (OCC)
 - 放电过流检测 (OCD)
 - 负载短路检测 (SCP)
- 针对电量耗尽电池的零电压充电
- 厂家设定的故障保护阈值
 - 故障检测电压阈值
 - 故障触发计时器
 - 故障恢复计时器
- 在电池充电器未启用时的运行模式
 - 正常模式 $I_{CC} = 4\mu\text{A}$
 - 关断 $I_q = 100\text{nA}$
- 运行温度范围 $T_A = -40^\circ\text{C}$ 至 $+85^\circ\text{C}$
- 封装:
 - 6 引脚 DSE (1.50mm x 1.50mm x 0.75mm)

2 应用

- 平板电脑
- 手机
- 手持式数据终端

3 说明

bq2970 电池保护器件会提供精确的监控和触发阈值，可在充电/放电电流较高或电池过充情况下提供过流保护。

bq2970 器件提供针对锂离子/锂聚合物电池的保护功能，并且监控外部功率 FET，以便在高充电或放电电流时提供保护。此外，还有针对过度充电和电量耗尽电池的监控和保护。这些特性在正常模式运行中消耗的电流极少。

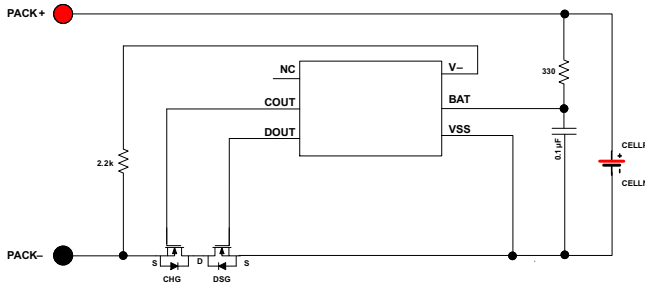
器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
bq2970、bq2971、bq2972、bq2973 ⁽²⁾	WSON (6)	1.50mm x 1.50mm

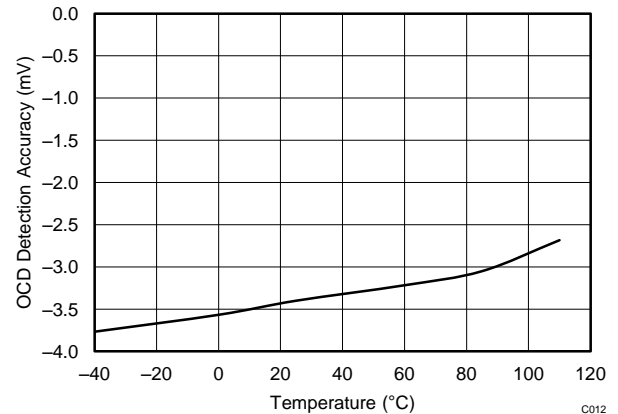
(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

(2) 如需了解已发行的器件，请参见 [器件比较表](#)。

简化原理图



OCD 检测准确度与温度之间的关系



C012



目录

1	特性	1	9	Detailed Description	15
2	应用	1	9.1	Overview	15
3	说明	1	9.2	Functional Block Diagram	16
4	修订历史记录	2	9.3	Feature Description	16
5	Device Comparison Table	3	9.4	Device Functional Modes	16
6	Pin Configuration and Functions	4	10	Application and Implementation	20
6.1	Pin Descriptions	4	10.1	Application Information	20
7	Specifications	5	10.2	Typical Application	20
7.1	Absolute Maximum Ratings	5	11	Power Supply Recommendations	23
7.2	ESD Ratings	5	12	Layout	23
7.3	Recommended Operating Conditions	5	12.1	Layout Guidelines	23
7.4	Thermal Information	5	12.2	Layout Example	23
7.5	DC Characteristics	6	13	器件和文档支持	24
7.6	Programmable Fault Detection Thresholds	6	13.1	相关文档	24
7.7	Programmable Fault Detection Timer Ranges	7	13.2	相关链接	24
7.8	Typical Characteristics	7	13.3	社区资源	24
8	Parameter Measurement Information	11	13.4	商标	24
8.1	Timing Charts	11	13.5	静电放电警告	24
8.2	Test Circuits	13	13.6	术语表	24
8.3	Test Circuit Diagrams	15	14	机械、封装和可订购信息	24

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (May 2016) to Revision E	Page
• Changed <i>0-V Charging Function Enabled</i>	18
• Changed <i>0-V Charging Inhibit Function</i>	18

Changes from Revision C (March 2016) to Revision D	Page
• Changed bq29733 to Released in <i>Device Configuration Table</i>	3

Changes from Revision B (November, 2015) to Revision C	Page
• 添加了器件号 bq2971、bq2972 和 bq2973。将文档标题更改为 bq297xx	1
• Added bq29708~bq29733 to <i>Device Configuration Table</i> . Clarified recovery delay and moved info to footnote 2	3
• Changed UVP release voltage value based on 100mV hysteresis from UVP threshold	20
• 已添加 <i>相关链接</i> 表	24

Changes from Revision A (June, 2014) to Revision B	Page
• 将器件号更改为 bq2970	1
• 将 <i>相关链接</i> 表从 <i>器件和文档支持</i> 部分中删除	24

Changes from Original (March, 2014) to Revision A	Page
• 已更改 将文档中的部件号从“bq29700”更改为“bq297xy”	1
• 已添加 有关查看可订购产品附录和“已发行器件配置”表的说明	1
• Added <i>Device Configuration Table</i> for part numbers bq29700 through bq29707	3

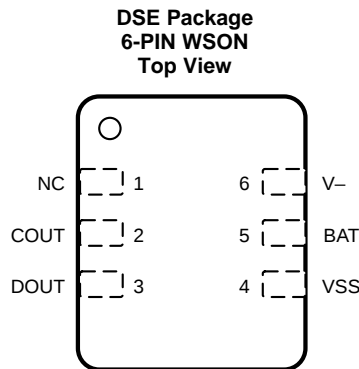
• Changed Terminal to Pin	4
• Added ohm symbol to value	6
• Changed "RANGE" to "CONDITION" and "ACCURACY" to "MIN, TYP, and MAX" column headings	6
• Added prefix "Factory Device Configuration:"	6
• Added Factory Programmable Options reference	15
• Added Factory Programmable Options table	15

5 Device Comparison Table

PART NUMBER ⁽¹⁾	OVP (V)	OVP DELAY (s)	UVP (V)	UVP DELAY (ms)	OCC (V)	OCC DELAY (ms)	OCD (V)	OCD DELAY (ms)	SCD (V)	SCD DELAY (µs)
bq29700	4.275	1.25	2.800	144	-0.100	8	0.100	20	0.5	250
bq29701	4.280	1.25	2.300	144	-0.100	8	0.125	8	0.5	250
bq29702	4.350	1	2.800	96	-0.155	8	0.160	16	0.3	250
bq29703	4.425	1.25	2.300	20	-0.100	8	0.160	8	0.5	250
bq29704	4.425	1.25	2.500	20	-0.100	8	0.125	8	0.5	250
bq29705	4.425	1.25	2.500	20	-0.100	8	0.150	8	0.5	250
bq29706	3.850	1.25	2.500	144	-0.150	8	0.200	8	0.6	250
bq29707	4.280	1	2.800	96	-0.090	6	0.090	16	0.3	250
bq29708 ⁽²⁾	4.350	0.25	2.300	20	-0.100	8	0.200	20	0.5	250
bq29709 ⁽²⁾	4.325	1.25	2.500	144	-0.100	8	0.150	8	0.5	250
bq29710 ⁽²⁾	4.300	1.25	2.300	144	-0.100	8	0.130	8	0.5	250
bq29711 ⁽²⁾	4.300	1.25	2.100	144	-0.100	8	0.130	8	0.5	250
bq29712 ⁽²⁾	4.350	1.25	2.300	20	-0.100	8	0.130	8	0.5	250
bq29713 ⁽²⁾	4.350	1.25	2.100	144	-0.100	8	0.120	8	0.5	250
bq29714 ⁽²⁾	4.350	1.25	2.100	144	-0.100	8	0.150	8	0.5	250
bq29715 ⁽²⁾	4.375	1.25	2.500	144	-0.100	8	0.120	20	0.5	250
bq29716	4.425	1.25	2.300	20	-0.100	8	0.165	8	0.5	250
bq29717	4.425	1.25	2.500	20	-0.100	8	0.130	8	0.5	250
bq29718	4.425	1.25	2.500	20	-0.100	8	0.100	8	0.5	250
bq29719 ⁽²⁾	4.425	1.25	2.800	20	-0.100	8	0.120	8	0.5	250
bq29720 ⁽²⁾	4.425	1.25	2.500	144	-0.100	8	0.100	8	0.5	250
bq29721 ⁽²⁾	4.425	1.25	2.500	144	-0.100	8	0.130	8	0.5	250
bq29722 ⁽²⁾	4.425	1	2.500	20	-0.100	8	0.100	8	0.5	250
bq29723	4.425	1	2.500	96	-0.060	4	0.100	8	0.3	250
bq29724 ⁽²⁾	4.425	1.25	2.500	20	-0.100	8	0.150	8	0.5	250
bq29725 ⁽²⁾	4.275	1.25	2.300	144	-0.100	8	0.100	8	0.5	250
bq29726 ⁽²⁾	4.280	1.25	2.300	144	-0.100	8	0.100	8	0.5	250
bq29727 ⁽²⁾	4.280	1.25	2.300	144	-0.100	8	0.130	8	0.5	250
bq29728 ⁽²⁾	4.280	1.25	2.800	144	-0.100	8	0.150	8	0.5	250
bq29729	4.275	1.25	2.300	20	-0.100	8	0.130	8	0.5	250
bq29730 ⁽²⁾	4.280	1.25	2.800	144	-0.100	8	0.100	8	0.5	250
bq29731 ⁽²⁾	4.280	1.25	2.800	144	-0.100	8	0.150	20	0.5	250
bq29732	4.280	1.25	2.500	144	-0.100	8	0.190	8	0.5	250
bq29733	4.400	1.25	2.800	20	-0.100	8	0.120	8	0.3	250
bq297xy	3.85 ~ 4.6	0.25, 1, 1.25, 4.5	2.0 ~ 2.8	20, 96, 125, 144	-0.045 ~ -0.155	4, 6, 8, 16	0.090 ~ 0.200	8, 16, 20, 48	0.3, 0.4, 0.5, 0.6	250

- (1) All the protections have a recovery delay time. The recovery timer starts as soon as the fault is triggered. The device will start to check for recovery condition only when the recovery timer expires. This is NOT a delay time between recovery condition to FETs recovery. OVP recovery delay = 12 ms; UVP/OCC/OCD recovery delay = 8 ms.
- (2) Product Preview only

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BAT	5	P	VDD pin
COUT	2	O	Gate Drive Output for Charge FET
DOUT	3	O	Gate Drive Output for Discharge FET
NC	1	NC	No Connection (electrically open, do <i>not</i> connect to BAT or VSS)
VSS	4	P	Ground pin
V-	6	I/O	Input pin for charger negative voltage

6.1 Pin Descriptions

6.1.1 Supply Input: BAT

This pin is the input supply for the device and is connected to the positive terminal of the battery pack. A 0.1- μ F input capacitor is connected to ground for filtering noise.

6.1.2 Cell Negative Connection: VSS

This pin is an input to the device for cell negative ground reference. Internal circuits associated with cell voltage measurements and overcurrent protection input to differential amplifier for either Vds sensing or external sense resistor sensing will be referenced to this node.

6.1.3 Voltage Sense Node: V-

This is a sense node used for measuring several fault detection conditions, such as overcurrent charging or overcurrent discharging configured as Vds sensing for protection. This input, in conjunction with VSS, forms the differential measurement for the stated fault detection conditions. A 2.2-k Ω resistor is connected between this input pin and Pack- terminal of the system in the application.

6.1.4 Discharge FET Gate Drive Output: DOUT

This pin is an output to control the discharge FET. The output is driven from an internal circuitry connected to the BAT supply. This output transitions from high to low when a fault is detected, and requires the DSG FET to turn OFF. A 5-M Ω high impedance resistor is connected from DOUT to VSS for gate capacitance discharge when the FET is turned OFF.

6.1.5 Charge FET Gate Drive Output: COUT

This pin is an output to control the charge FET. The output is driven from an internal circuitry connected to the BAT supply. This output transitions from high to low when a fault is detected, and requires the CHG FET to turn OFF. A 5-M Ω high impedance resistor is connected from COUT to Pack- for gate capacitance discharge when FET is turned OFF.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Supply control and input	Input voltage: BAT	-0.3	12	V
	V- pin(pack-)	BAT - 28	BAT + 0.3	V
FET drive and protection	DOUT (Discharge FET Output), GDSG (Discharge FET Gate Drive)	VSS - 0.3	BAT + 0.3	V
	COUT (Charge FET Output), GCHG (Charge FET Gate Drive)	BAT - 28	BAT + 0.3	V
	Operating temperature: T _{FUNC}	-40	85	°C
Storage temperature, T _{stg}		-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _{ESD} ⁽¹⁾	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽²⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽³⁾	±500
			V

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 1000 V can have higher performance.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V can have higher performance.

7.3 Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
Supply control and input	Positive input voltage: BAT	-0.3	8	V
	Negative input voltage: V-	BAT - 25	BAT	V
FET drive and protection	Discharge FET control: DOUT	VSS	BAT	V
	Charge FET control: COUT	BAT - 25	BAT	V
Temperature Ratings	Operating temperature: T _{Amb}	-40	85	°C
	Storage temperature: T _S	-55	150	°C
	Lead temperature (soldering 10 s)		300	°C
	Thermal resistance junction to ambient, θ_{JA} ⁽¹⁾		250	°C/W

- (1) For more information about traditional and new thermal metrics, see the IC package Thermal Metrics application report, [SPRA953](#).

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		bq297xx	
		DSE (WSON)	
		12 PINS	
			UNIT
R _{θJA, High K}	Junction-to-ambient thermal resistance	190.5	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	94.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	149.3	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	6.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	152.8	°C/W
R _{θJC(bottom)}	Junction-to-case(bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 DC Characteristics

Typical Values stated where $T_A = 25^\circ\text{C}$ and $BAT = 3.6\text{ V}$. Min/Max values stated where $T_A = -40^\circ\text{C}$ to 85°C , and $BAT = 3\text{ V}$ to 4.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption						
V_{BAT}	Device operating range	$BAT - VSS$	1.5		8	V
		$BAT - V-$	1.5		28	
I_{NORMAL}	Current consumption in NORMAL mode	$BAT = 3.8\text{ V}$, $V- = 0\text{ V}$		4	5.5	μA
I_{Power_down}	Current consumption in power down mode	$BAT = V- = 1.5\text{ V}$			0.1	μA
FET Output, DOUT and COUT						
V_{OL}	Charge FET low output	$I_{OL} = 30\ \mu\text{A}$, $BAT = 3.8\text{ V}$		0.4	0.5	V
V_{OH}	Charge FET high output	$I_{OH} = -30\ \mu\text{A}$, $BAT = 3.8\text{ V}$	3.4	3.7		V
V_{OL}	Discharge FET low output	$I_{OL} = 30\ \mu\text{A}$, $BAT = 2\text{ V}$		0.2	0.5	V
V_{OH}	Discharge FET high output	$I_{OH} = -30\ \mu\text{A}$, $BAT = 3.8\text{ V}$	3.4	3.7		V
Pullup Internal Resistance on V-						
R_{V-D}	Resistance between V- and VBAT	$V_{BAT} = 1.8\text{ V}$, $V- = 0\text{ V}$	100	300	550	k Ω
Current sink on V-						
I_{V-S}	Current sink on V- to VSS	$V_{BAT} = 3.8\text{ V}$	8		24	μA
Load short detection on V-						
V_{short}	Short detection voltage	$V_{BAT} = 3.8\text{ V}$ and $R_{PackN} = 2.2\text{ k}\Omega$		$\frac{V_{BAT} - 1\text{ V}}{1}$		V
0-V battery charge function						
V_{0CHG}	0-V battery charging start voltage	0-V battery charging function allowed	1.7			V
0-V battery charge inhibit function						
V_{0INH}	0-V battery charging inhibit voltage threshold	0-V battery charging function disallowed			0.75	V

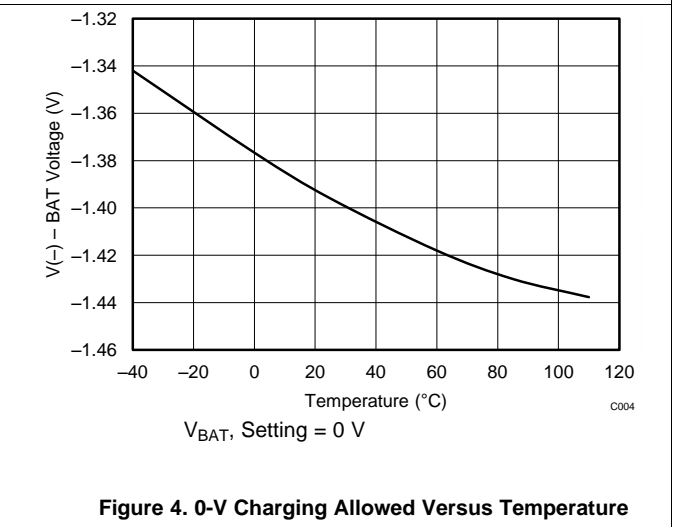
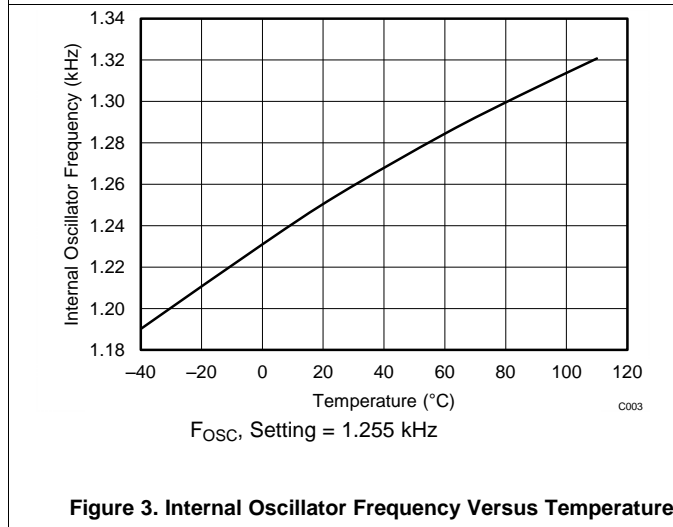
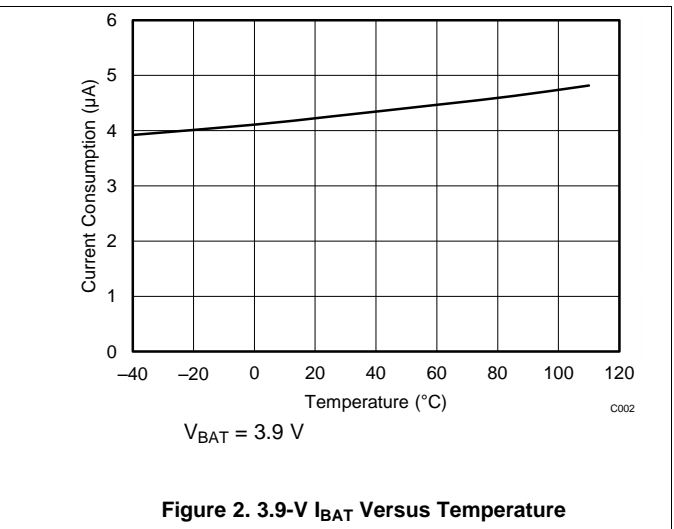
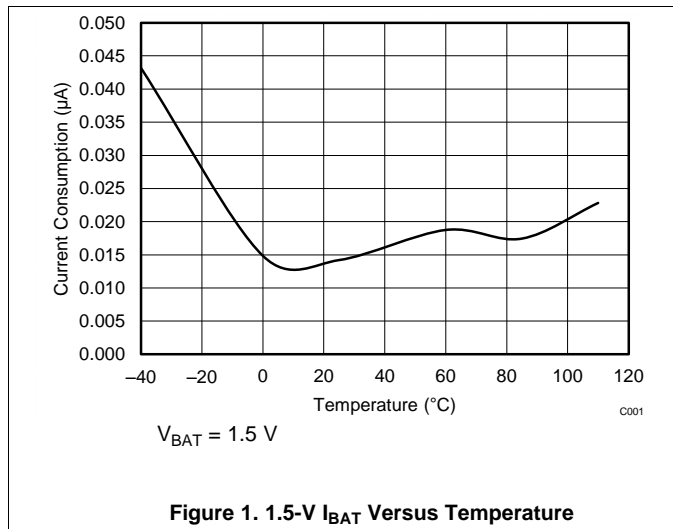
7.6 Programmable Fault Detection Thresholds

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
V_{OVP}	Overcharge detection voltage	Factory Device Configuration: 3.85 V to 4.60 V in 50-mV steps	$T_A = 25^\circ\text{C}$	-10	10	mV
			$T_A = 0^\circ\text{C}$ to 60°C	-20	20	mV
$V_{OVP-Hys}$	Overcharge release hysteresis voltage	100 mV and $(VSS - V-) > OCC$ (min) for release, $T_A = 25^\circ\text{C}$	-20		20	mV
V_{UVP}	Over-discharge detection voltage	Factory Device Configuration: 2.00 V to 2.80 V in 50-mV steps, $T_A = 25^\circ\text{C}$	-50		50	mV
$V_{UVP+Hys}$	Over-discharge release hysteresis voltage	100 mV and $(BAT - V-) > 1\text{ V}$ for release, $T_A = 25^\circ\text{C}$	-50		50	mV
V_{OCD}	Discharging overcurrent detection voltage	Factory Device Configuration: 90 mV to 200 mV in 5-mV steps	$T_A = 25^\circ\text{C}$	-10	10	mV
			$T_A = -40^\circ\text{C}$ to 85°C	-15	15	mV
Release of V_{OCD}	Release of discharging overcurrent detection voltage	Release when $BAT - V- > 1\text{ V}$		1		V
V_{OCC}	Charging overcurrent detection voltage	Factory Device Configuration: -45 mV to -155 mV in 5-mV steps	$T_A = 25^\circ\text{C}$	-10	10	mV
			$T_A = -40^\circ\text{C}$ to 85°C	-15	15	mV
Release of V_{OCC}	Release of overcurrent detection voltage	Release when $VSS - V- \geq OCC$ (min)		40		mV
V_{SCC}	Short Circuit detection voltage	Factory Device Configuration: 300 mV, 400 mV, 500 mV, 600 mV	$T_A = 25^\circ\text{C}$	-100	100	mV
V_{SCCR}	Release of Short Circuit detection voltage	Release when $BAT - V- \geq 1\text{ V}$		1		V

7.7 Programmable Fault Detection Timer Ranges

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
t _{OVPD}	Overcharge detection delay time	Factory Device Configuration: 0.25 s, 1 s, 1.25 s, 4.5 s			s
t _{UVPD}	Over-discharge detection delay time	Factory Device Configuration: 20 ms, 96 ms, 125 ms, 144 ms			ms
t _{OCCD}	Discharging overcurrent detection delay time	Factory Device Configuration: 8 ms, 16 ms, 20 ms, 48 ms			ms
t _{OCCD}	Charging overcurrent detection delay time	Factory Device Configuration: 4 ms, 6 ms, 8 ms, 16 ms			ms
t _{SCCD}	Short Circuit detection delay time	250 μs (fixed)			μs

7.8 Typical Characteristics



Typical Characteristics (continued)

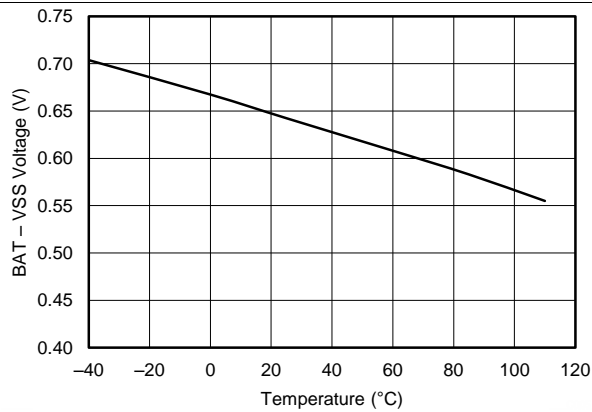


Figure 5. 0-V Charging Disallowed Versus Temperature

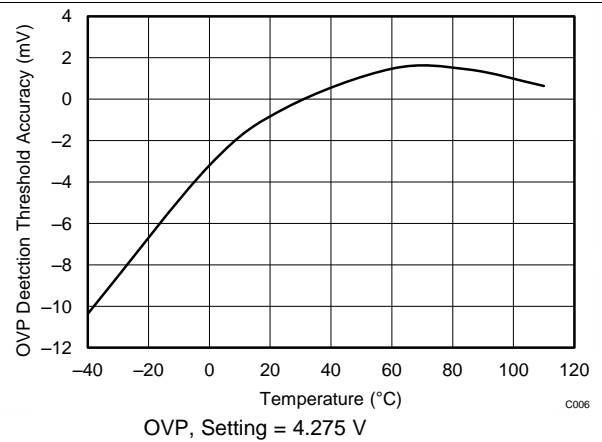


Figure 6. OVP Detection Accuracy Versus Temperature

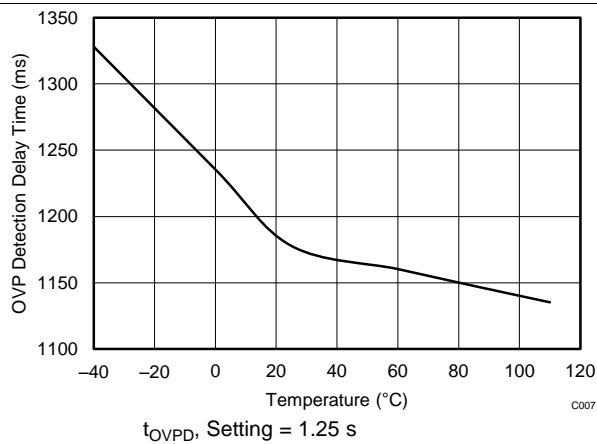


Figure 7. OVP Detection Delay Time Versus Temperature

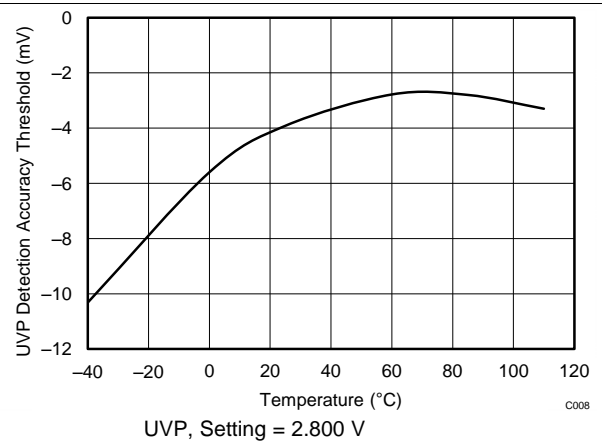


Figure 8. UVP Detection Accuracy Versus Temperature

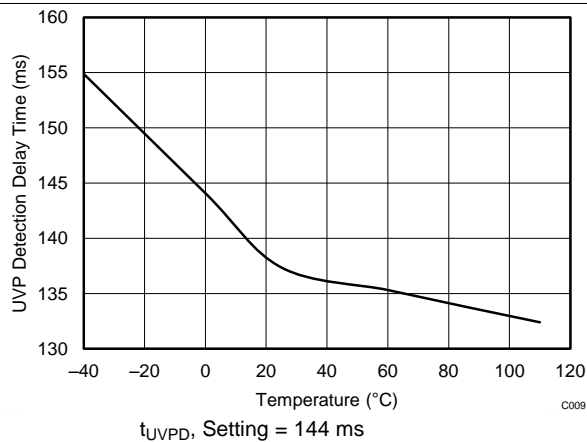


Figure 9. UVP Detection Delay Time Versus Temperature

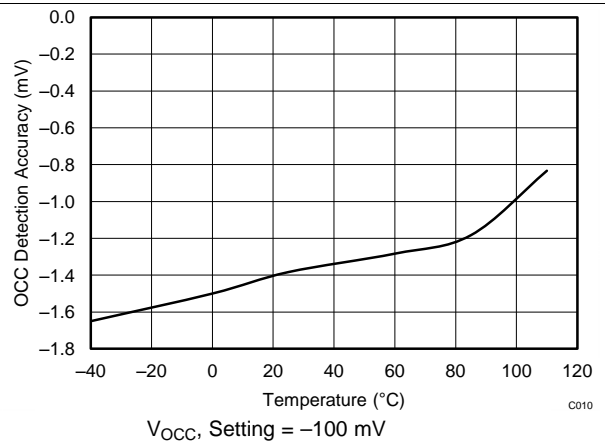
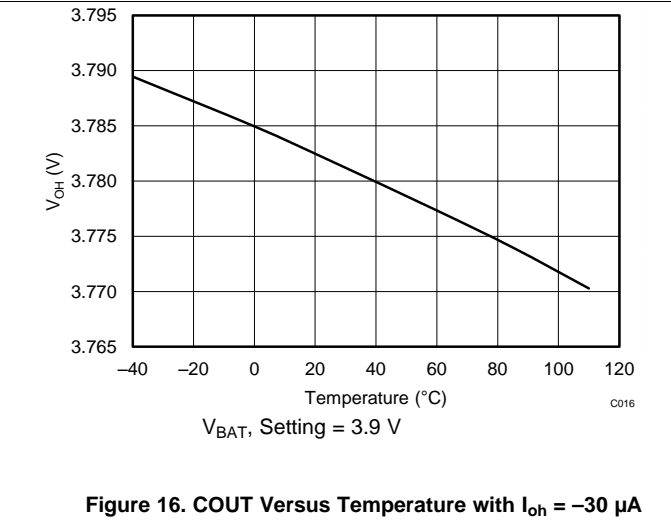
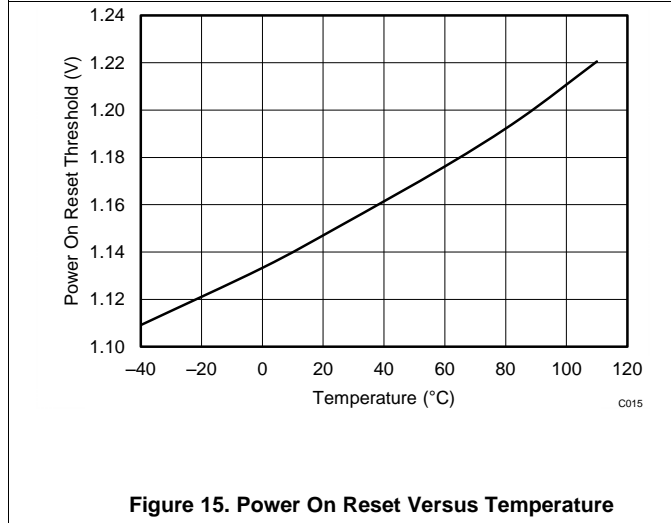
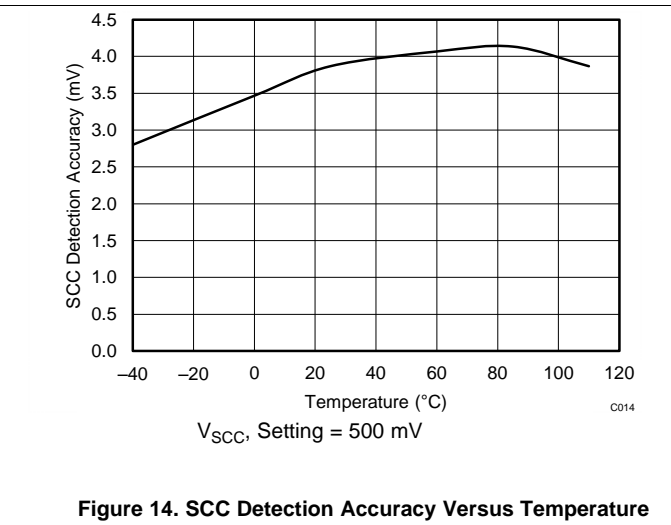
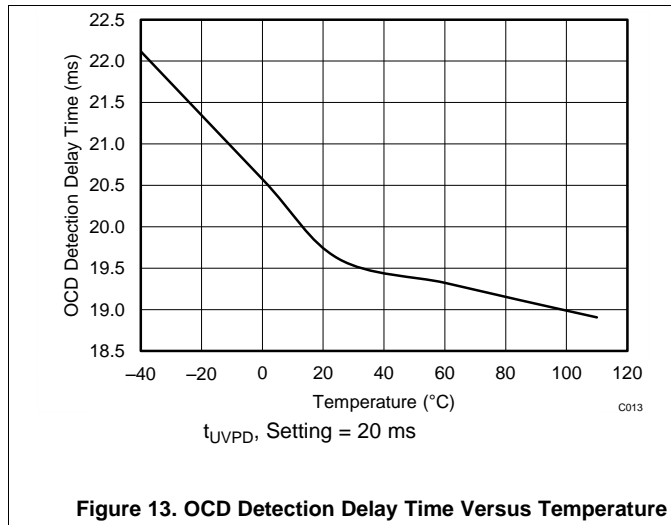
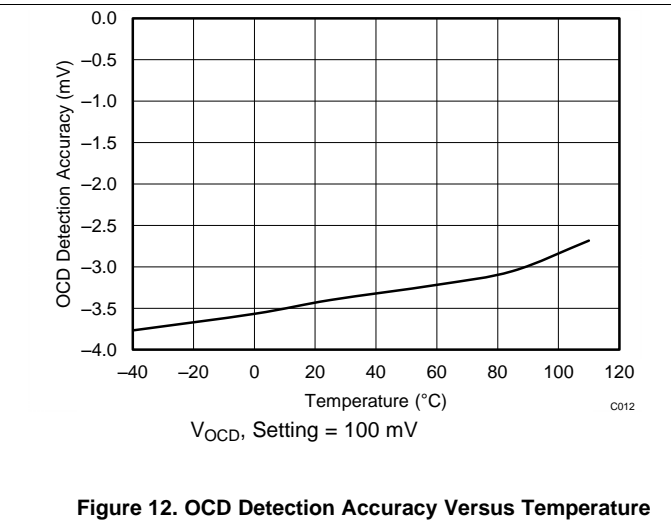
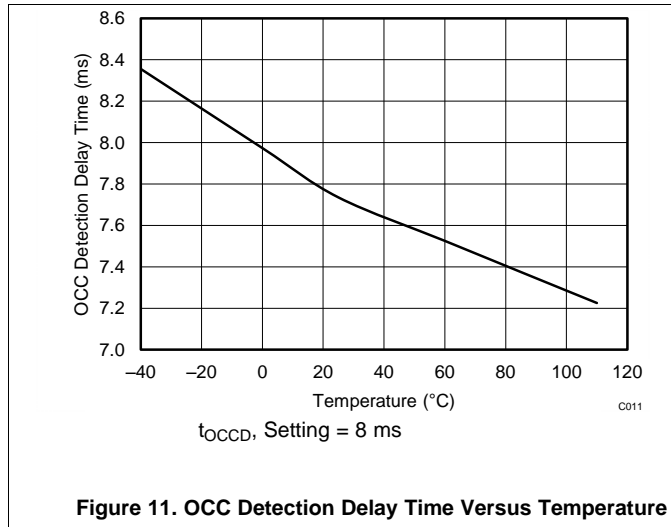


Figure 10. OCC Detection Accuracy Versus Temperature

Typical Characteristics (continued)



Typical Characteristics (continued)

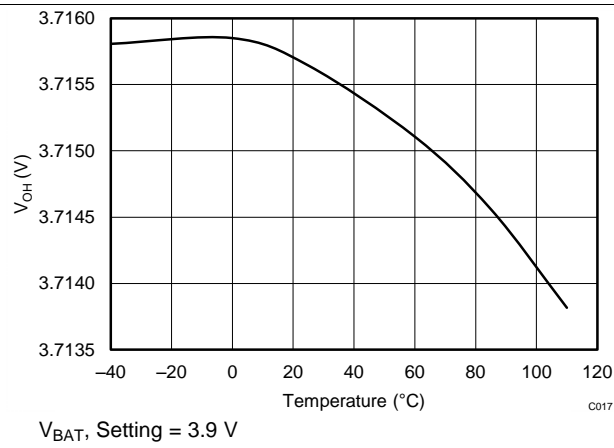


Figure 17. DOUT Versus Temperature with $I_{oh} = -30 \mu A$

8 Parameter Measurement Information

8.1 Timing Charts

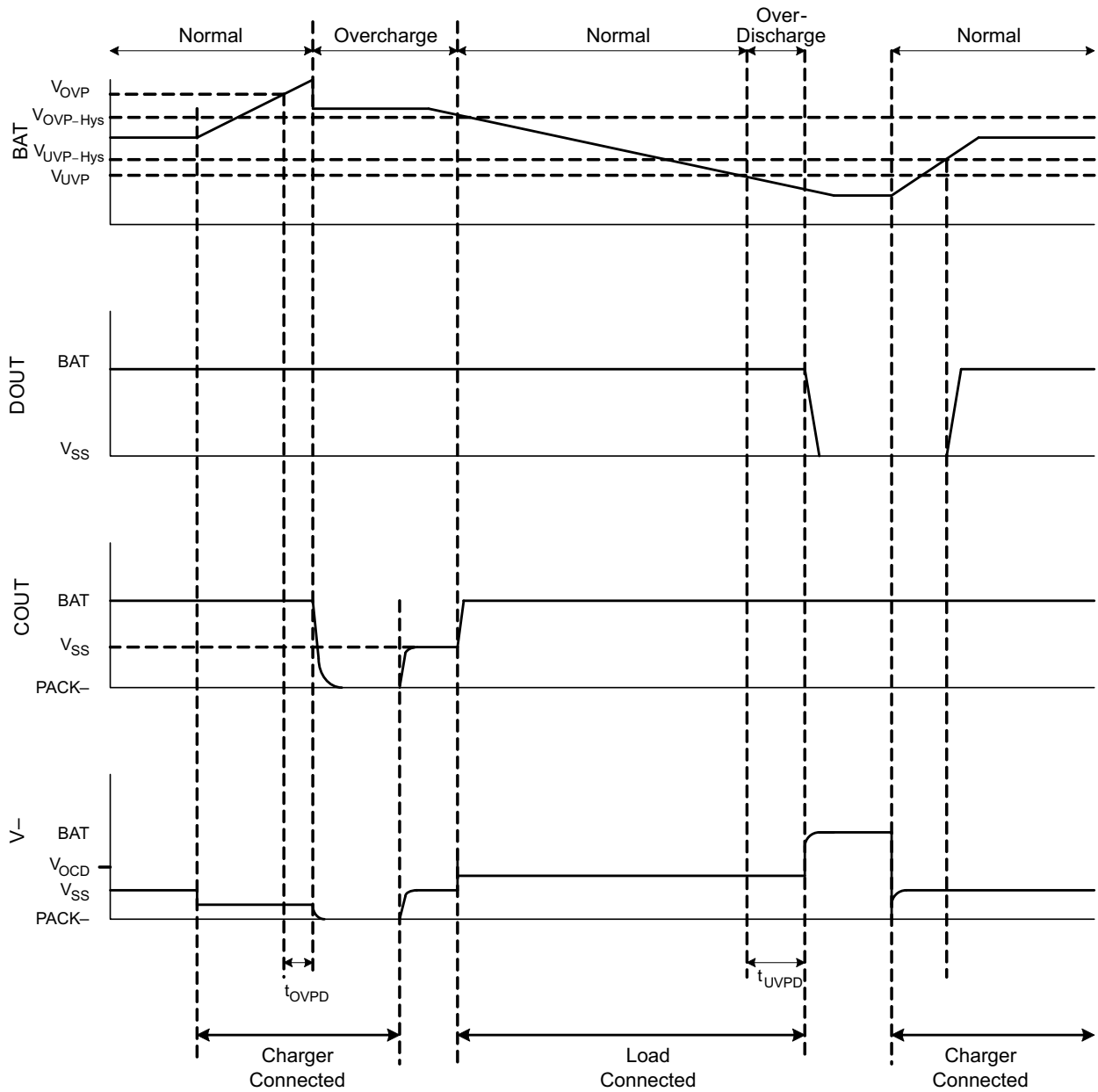


Figure 18. Overcharge Detection, Over-Discharge Detection

Timing Charts (continued)

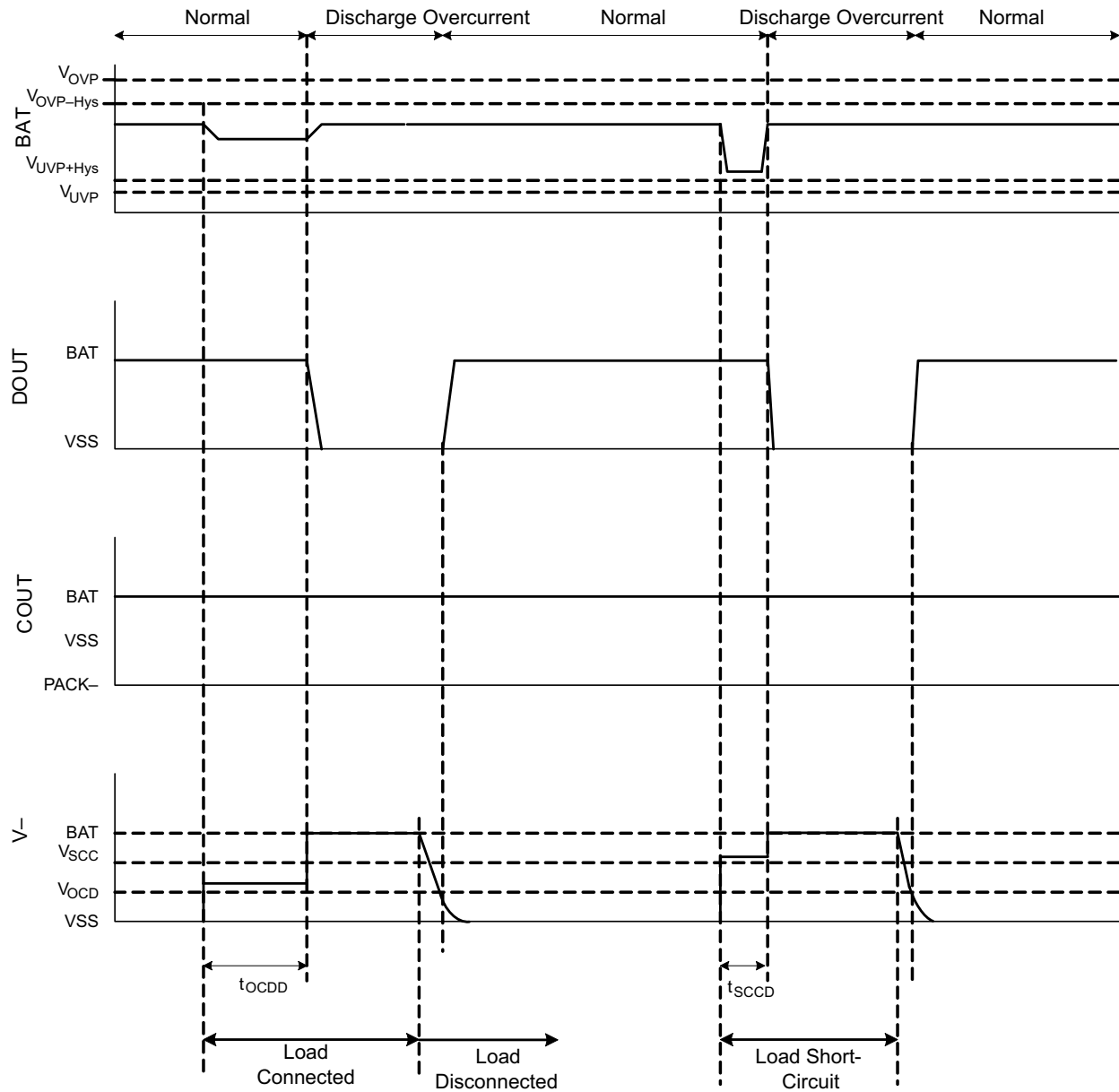


Figure 19. Discharge Overcurrent Detection

8.2 Test Circuits

The following tests are referenced as follows: The COUT and DOUT outputs are “H,” which are higher than the threshold voltage of the external logic level FETs and regarded as ON state. “L” is less than the turn ON threshold for external NMOS FETs and regarded as OFF state. The COUT pin is with respect to V–, and the DOUT pin is with respect to VSS.

1. **Overcharge detection voltage and overcharge release voltage (Test Circuit 1):**

The overcharge detection voltage (V_{OVP}) is measured between the BAT and VSS pins, respectively. Once V1 is increased, the over-detection is triggered, and the delay timer expires. Then, COUT transitions from a high to low state and reduces the V1 voltage to check for the overcharge hysteresis parameter ($V_{OVP-HYS}$). The delta voltage between overcharge detection voltages (V_{OVP}) and the overcharge release occurs when the CHG FET drive output goes from low to high.

2. **Over-discharge detection voltage and over-discharge release voltage (Test Circuit 2):**

Over-discharge detection (V_{UVP}) is defined as the voltage between BAT and VSS at which the DSG drive output goes from high to low by reducing the V1 voltage. V1 is set to 3.5 V and gradually reduced while V2 is set to 0 V. The over-discharge release voltage is defined as the voltage between BAT and VSS at which the DOUT drive output transition from low to high when V1 voltage is gradually increased from a V_{UVP} condition. The overcharge hysteresis voltage is defined as the delta voltage between V_{UVP} and the instance at which the DOUT output drive goes from low to high.

3. **Discharge overcurrent detection voltage (Test Circuit 2):**

The discharge overcurrent detection voltage (V_{OCD}) is measured between V– and VSS pins and triggered when the V2 voltage is increased above V_{OCD} threshold with respect to VSS. This delta voltage once satisfied will trigger an internal timer t_{OCD} before the DOUT output drive transitions from high to low.

4. **Load short circuit detection voltage (Test Circuit 2):**

Load short-circuit detection voltage (V_{SCC}) is measured between V– and VSS pins and triggered when the V2 voltage is increased above V_{SCC} threshold with respect to VSS within 10 μ s. This delta voltage, once satisfied, triggers an internal timer t_{SCC} before the DOUT output drive transitions from high to low.

5. **Charge overcurrent detection voltage (Test Circuit 2):**

The charge overcurrent detection voltage (V_{OCC}) is measured between VSS and V– pins and triggered when the V2 voltage is increased above V_{OCC} threshold with respect to V–. This delta voltage, once satisfied, triggers an internal timer t_{OCC} before the COUT output drive transitions from high to low.

6. **Operating current consumption (Test Circuit 2):**

The operating current consumption $I_{BNORMAL}$ is the current measured going into the BAT pin under the following conditions: V1 = 3.9 V and V2 = 0 V.

7. **Power down current consumption (Test Circuit 2):**

The operating current consumption I_{Power_down} is the current measured going into the BAT pin under the following conditions: V1 = 1.5 V and V2 = 1.5 V.

8. **Resistance between V– and BAT pin (Test Circuit 3):**

Measure the resistance (R_{V_D}) between V– and BAT pins by setting the following conditions: V1 = 1.8 V and V2 = 0 V.

9. **Current sink between V– and VSS (Test Circuit 3):**

Measure the current sink I_{V_S} between V– and VSS pins by setting the following condition: V1 = 4 V.

10. **COUT current source when activated High (Test Circuit 4):**

Measure I_{COUT} current source on the COUT pin by setting the following conditions: V1 = 3.9 V, V2 = 0 V, and V3 = 3.4 V.

11. **COUT current sink when activated Low (Test Circuit 4):**

Measure I_{COUT} current sink on COUT pin by setting the following conditions: V1 = 4.5 V, V2 = 0 V, and V3 = 0.5 V.

Test Circuits (continued)
12. DOUT current source when activated High (Test Circuit 4):

Measure I_{DOUT} current source on DOUT pin by setting the following conditions: $V1 = 3.9\text{ V}$, $V2 = 0\text{ V}$, and $V3 = 3.4\text{ V}$.

13. DOUT current sink when activated Low (Test Circuit 4):

Measure I_{DOUT} current sink on DOUT pin by setting the following conditions: $V1 = 2.0\text{ V}$, $V2 = 0\text{ V}$, and $V3 = 0.4\text{ V}$.

14. Overcharge detection delay (Test Circuit 5):

The overcharge detection delay time t_{OVDP} is the time delay before the COUT drive output transitions from high to low once the voltage on $V1$ exceeds the V_{OVP} threshold. Set $V2 = 0\text{ V}$ and then increase $V1$ until BAT input exceeds the V_{OVP} threshold, then check the time for when COUT goes from high to low.

15. Over-discharge detection delay (Test Circuit 5):

The over-discharge detection delay time t_{UVPD} is the time delay before the DOUT drive output transitions from high to low once the voltage on $V1$ decreases to V_{UVP} threshold. Set $V2 = 0\text{ V}$ and then decrease $V1$ until BAT input reduces to the V_{UVP} threshold, then check the time of when DOUT goes from high to low.

16. Discharge overcurrent detection delay (Test Circuit 5):

The discharge overcurrent detection delay time t_{OCDD} is the time for DOUT drive output to transition from high to low after the voltage on $V2$ is increased from 0 V to 0.35 V . $V1 = 3.5\text{ V}$ and $V2$ starts from 0 V and increases to trigger threshold.

17. Load short circuit detection delay (Test Circuit 5):

The load short-circuit detection delay time t_{SCDD} is the time for DOUT drive output to transition from high to low after the voltage on $V2$ is increased from 0 V to $V1 - 1\text{ V}$. $V1 = 3.5\text{ V}$ and $V2$ starts from 0 V and increases to trigger threshold.

18. Charge overcurrent detection delay (Test Circuit 5):

The charge overcurrent detection delay time t_{OCCD} is the time for COUT drive output to transition from high to low after the voltage on $V2$ is decreased from 0 V to -0.3 V . $V1 = 3.5\text{ V}$ and $V2$ starts from 0 V and decreases to trigger threshold.

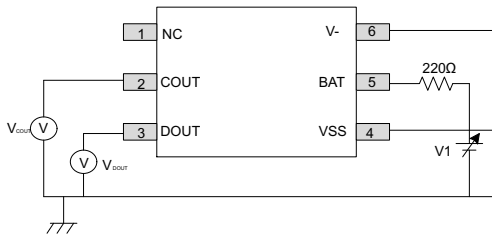
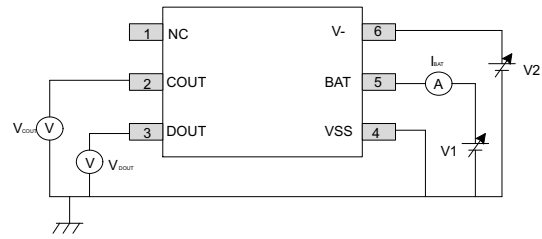
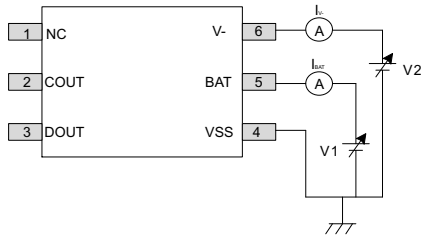
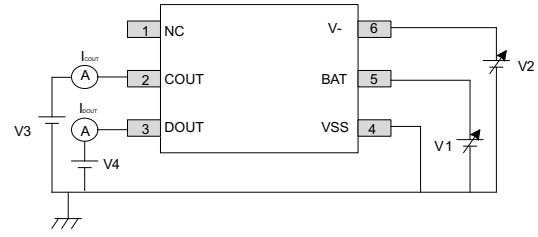
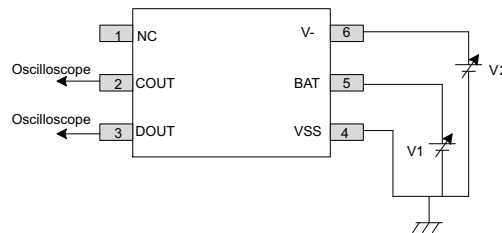
19. 0-V battery charge starting charger voltage (Test Circuit 2):

The 0-V charge for start charging voltage V_{OCHA} is defined as the voltage between BAT and $V-$ pins at which COUT goes high when voltage on $V2$ is gradually decreased from a condition of $V1 = V2 = 0\text{ V}$.

20. 0-V battery charge inhibition battery voltage (Test Circuit 2):

The 0-V charge inhibit for charger voltage V_{OINH} is defined as the voltage between BAT and VSS pins at which COUT should go low as $V1$ is gradually decreased from $V1 = 2\text{ V}$ and $V2 = -4\text{ V}$.

8.3 Test Circuit Diagrams


Figure 20. Test Circuit 1

Figure 21. Test Circuit 2

Figure 22. Test Circuit 3

Figure 23. Test Circuit 4

Figure 24. Test Circuit 5

9 Detailed Description

9.1 Overview

This bq2970 device is a primary protector for a single-cell Li-Ion/Li-Polymer battery pack. The device uses a minimum number of external components to protect for overcurrent conditions due to high discharge/charge currents in the application. In addition, it monitors and helps to protect against battery pack overcharging or depletion of energy in the pack. The bq2970 device is capable of having an input voltage of 8 V from a charging adapter and can tolerate a voltage of BAT – 25 V across the two input pins. In the condition when a fault is triggered, there are timer delays before the appropriate action is taken to turn OFF either the CHG or DSG FETs. The recovery period also has a timer delay once the threshold for recovery condition is satisfied. These parameters are fixed once they are programmed. There is also a feature called zero voltage charging that enables depleted cells to be charged to an acceptable level before the battery pack can be used for normal operation. Zero voltage charging is allowed if the charger voltage is above 1.7 V. For Factory Programmable Options, see [Table 1](#).

Table 1. Factory Programmable Options

PARAMETER	FACTORY DEVICE CONFIGURATION	
V _{OVP}	Overcharge detection voltage	3.85 V to 4.60 V in 50-mV steps
V _{UVP}	Over-discharge detection voltage	2.00 V to 2.80 V in 50-mV steps
V _{OCD}	Discharging overcurrent detection voltage	90 mV to 200 mV in 5-mV steps
V _{OCC}	Charging overcurrent detection voltage	–45 mV to –155 mV in 5-mV steps
V _{SCC}	Short Circuit detection voltage	300 mV, 400 mV, 500 mV, 600 mV
t _{OVPD}	Overcharge detection delay time	0.25 s, 1.00 s, 1.25 s, 4.50 s
t _{UVPD}	Over-discharge detection delay time	20 ms, 96 ms, 125 ms, 144 ms
t _{OCDD}	Discharging overcurrent detection delay time	8 ms, 16 ms, 20 ms, 48 ms

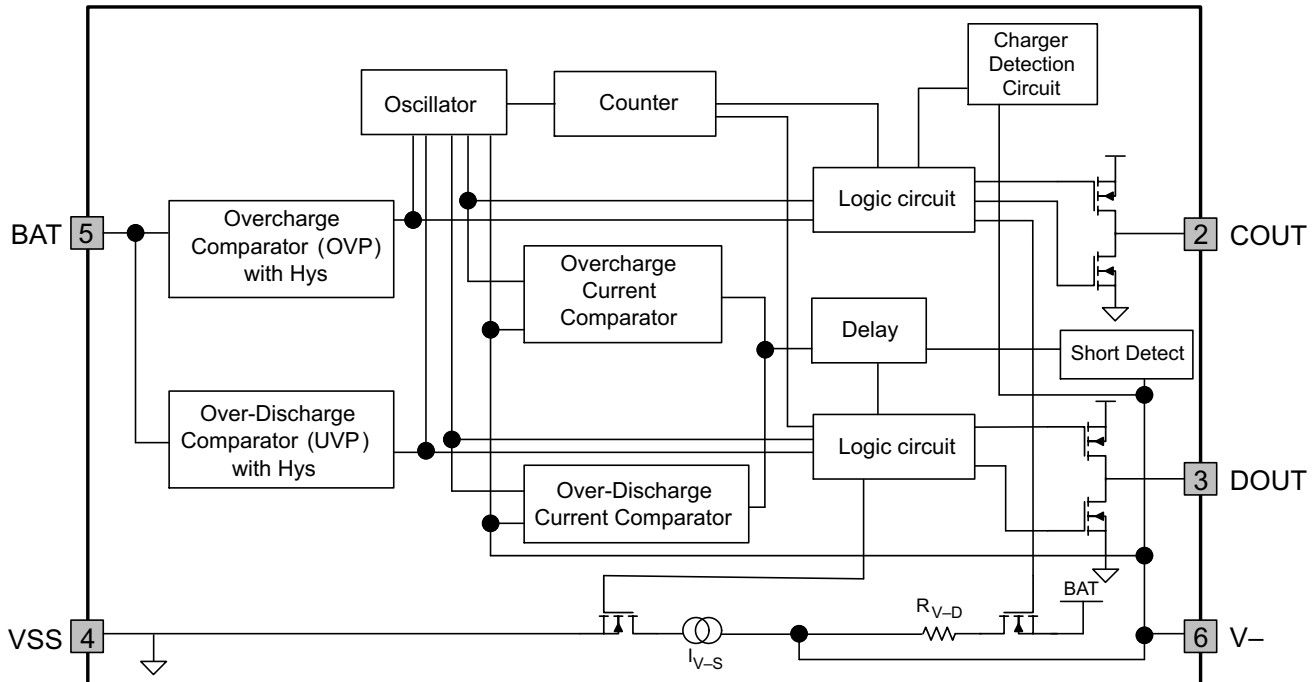
Overview (continued)

Table 1. Factory Programmable Options (continued)

PARAMETER		FACTORY DEVICE CONFIGURATION
t_{OCCD}	Charging overcurrent detection delay time	4 ms, 6 ms, 8 ms, 16 ms
t_{SCCD}	Short Circuit detection delay time	250 μ s (fixed)

For available released devices, see the [Released Device Configurations](#) table.

9.2 Functional Block Diagram



9.3 Feature Description

The bq2970 family of devices measures voltage drops across several input pins for monitoring and detection of the following faults: OCC, OCD, OVP, and UVP. An internal oscillator initiates a timer to the fixed delays associated with each parameter once the fault is triggered. Once the timer expires due to a fault condition, the appropriate FET drive output (COUT or DOUT) is activated to turn OFF the external FET. The same method is applicable for the recovery feature once the system fault is removed and the recovery parameter is satisfied, then the recovery timer is initiated. If there are no reoccurrences of this fault during this period, the appropriate gate drive is activated to turn ON the appropriate external FET.

9.4 Device Functional Modes

9.4.1 Normal Operation

This device monitors the voltage of the battery connected between BAT pin and VSS pin and the differential voltage between V- pin and VSS pin to control charging and discharging. The system is operating in NORMAL mode when the battery voltage range is between the over-discharge detection threshold (V_{UVP}) and the overcharge detection threshold (V_{OVP}), and the V- pin voltage is within the range for charge overcurrent threshold (V_{OCC}) to over-discharge current threshold (V_{OCD}) when measured with respect to VSS. If these conditions are satisfied, the device turns ON the drive for COUT and DOUT FET control.

Device Functional Modes (continued)

CAUTION

When the battery is connected for the first time, the discharging circuit might not be enabled. In this case, short the V– pin to the VSS pin.

Alternatively, connect the charger between the Pack+ and Pack– terminals in the system.

9.4.2 Overcharge Status

This mode is detected when the battery voltage measured is higher than the overcharge detection threshold (V_{OVP}) during charging. If this condition exists for a period greater than the overcharge detection delay (t_{OVPD}) or longer, the COUT output signal is driven low to turn OFF the charging FET to prevent any further charging of the battery.

The overcharge condition is released if one of the following conditions occurs:

- If the V– pin is higher than the overcharge detection voltage (V_{OCC_Min}), the device releases the overcharge status when the battery voltage drops below the overcharge release voltage ($V_{OVP-Hys}$).
- If the V– pin is higher than or equal to the over-discharge detection voltage (V_{OCD}), the device releases the overcharge status when the battery voltage drops below the overcharge detection voltage (V_{OVP}).

The discharge is initiated by connecting a load after the overcharge detection. The V– pin rises to a voltage greater than VSS due to the parasitic diode of the charge FET conducting to support the load. If the V– pin voltage is higher than or equal to the discharge overcurrent detection threshold (V_{OCD}), the overcurrent condition status is released only if the battery voltage drops lower than or equal to the overcharge detection voltage (V_{OVP}).

CAUTION

1. If the battery is overcharged to a level greater than overcharge detection (V_{OVP}) and the battery voltage does *not* drop below the overcharge detection voltage (V_{OVP}) with a heavy load connected, the discharge overcurrent and load short-circuit detection features do *not* function until the battery voltage drops below the overcharge detection voltage (V_{OVP}). The internal impedance of a battery is in the order of tens of $m\Omega$, so application of a heavy load on the output should allow the battery voltage to drop immediately, enabling discharge overcurrent detection and load short-circuit detection features after an overcharge release delay.
2. When a charger is connected after an overcharge detection, the overcharge status does *not* release even if the battery voltage drops below the overcharge release threshold. The overcharge status is released when the V– pin voltage exceeds the overcurrent detection voltage (V_{OCD}) by removing the charger.

9.4.3 Over-Discharge Status

If the battery voltage drops below the over-discharge detection voltage (V_{UVP}) for a time greater than (t_{UVPD}) the discharge control output, DOUT is switched to a low state and the discharge FET is turned OFF to prevent further discharging of the battery. This is referred to as an over-discharge detection status. In this condition, the V– pin is internally pulled up to BAT by the resistor R_{V-D} . When this occurs, the voltage difference between V– and BAT pins is 1.3 V or lower, and the current consumption of the device is reduced to power-down level $I_{STANDBY}$. The current sink I_{V-S} is not active in power-down state or over-discharge state. The power-down state is released when a charger is connected and the voltage delta between V– and BAT pins is greater than 1.3 V.

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is lower than -0.7 V, the device releases the over-discharge state and allows the DOUT pin to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection voltage (V_{UVP}).

If a charger is connected to a battery in over-discharge state and the voltage detected at the V– is higher than -0.7 V, the device releases the over-discharge state and allows the DOUT pin to go high and turn ON the discharge FET once the battery voltage exceeds over-discharge detection release hysteresis voltage ($V_{UVP+Hys}$).

Device Functional Modes (continued)

9.4.4 Discharge Overcurrent Status (Discharge Overcurrent, Load Short-Circuit)

When a battery is in normal operation and the V^- pin is equal to or higher than the discharge overcurrent threshold for a time greater than the discharge overcurrent detection delay, the DOUT pin is pulled low to turn OFF the discharge FET and prevent further discharge of the battery. This is known as the discharge overcurrent status. In the discharge overcurrent status, the V^- and VSS pins are connected by a constant current sink I_{V-S} . When this occurs and a load is connected, the V^- pin is at BAT potential. If the load is disconnected, the V^- pin goes to VSS (BAT/2) potential.

This device detects the status when the impedance between Pack+ and Pack- (see Figure 26) increases and is equal to the impedance that enables the voltage at the V^- pin to return to $BAT - 1\text{ V}$ or lower. The discharge overcurrent status is restored to the normal status.

Alternatively, by connecting the charger to the system, the device returns to normal status from discharge overcurrent detection status, because the voltage at the V^- pin drops to $BAT - 1\text{ V}$ or lower.

The resistance R_{V-D} between V^- and BAT is not connected in the discharge overcurrent detection status.

9.4.5 Charge Overcurrent Status

When a battery is in normal operation status and the voltage at V^- pin is lower than the charge overcurrent detection due to high charge current for a time greater than charge overcurrent detection delay, the COUT pin is pulled low to turn OFF the charge FET and prevent further charging to continue. This is known as charge overcurrent status.

The device is restored to normal status from charge overcurrent status when the voltage at the V^- pin returns to charge overcurrent detection voltage or higher by removing the charger from the system.

The charge overcurrent detection feature does *not* work in the over-discharge status.

The resistance R_{V-D} between V^- and BAT and the current sink I_{V-S} is not connected in the charge overcurrent status.

9.4.6 0-V Charging Function Enabled

This feature enables recharging a connected battery that has very low voltage due to self-discharge. When the charger applies a voltage greater than or equal to V_{0CHG} to Pack+ and Pack- connections, the COUT pin gate drive is fixed by the BAT pin voltage.

Once the voltage between the gate and the source of the charging FET becomes equal to or greater than the turn ON voltage due to the charger voltage, the charging FET is ON and the battery is charged with current flow through the charging FET and the internal parasitic diode of the discharging FET. Once the battery voltage is equal to or higher than the over-discharge release voltage, the device enters normal status.

CAUTION

1. Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to have the 0-V battery charger function.
2. The 0-V battery charge feature has a higher priority than the charge overcurrent detection function. In this case, the 0-V charging will be allowed and the battery charges forcibly, which results in charge overcurrent detection being disabled if the battery voltage is lower than the over-discharge detection voltage.

9.4.7 0-V Charging Inhibit Function

This feature inhibits recharging a battery that has an internal short circuit of a 0-V battery. If the battery voltage is below the charge inhibit voltage V_{0INH} or lower, the charge FET control gate is fixed to the Pack- voltage to inhibit charging. When the battery is equal to V_{0INH} or higher, charging can be performed. The 0-V charge inhibit function is available in all configurations of the bq297xx device.

Device Functional Modes (continued)

CAUTION

Some battery providers do not recommend charging a depleted (self-discharged) battery. Consult the battery supplier to determine whether to enable or inhibit the 0-V battery charger function.

9.4.8 Delay Circuit

The detection delay timers are based from an internal clock with a frequency of 10 kHz.

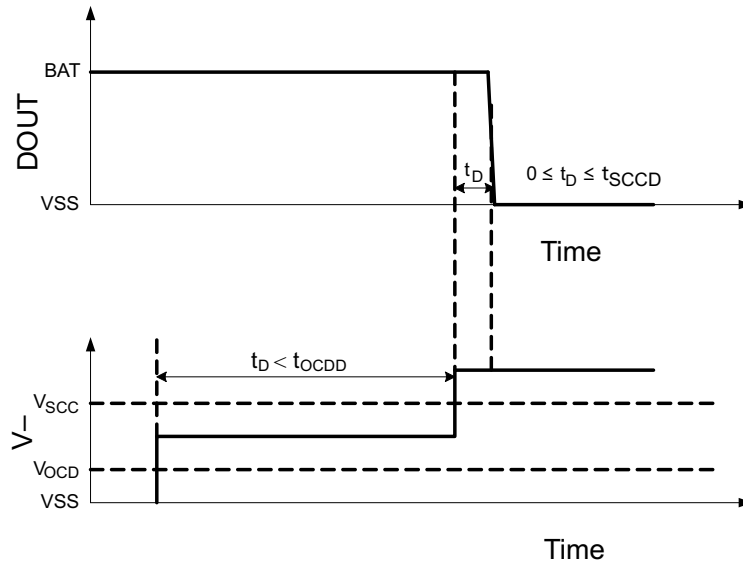


Figure 25. Delay Circuit

If the over-discharge current is detected, but remains below the over-discharge short circuit detection threshold, the over-discharge detection conditions must be valid for a time greater than or equal to over-discharge current delay t_{OCCD} time before the DOUT goes low to turn OFF the discharge FET. However, during any time the discharge overcurrent detection exceeds the short circuit detection threshold for a time greater than or equal to load circuit detection delay t_{SCCD} , the DOUT pin goes low in a faster delay for protection.

10 Application and Implementation

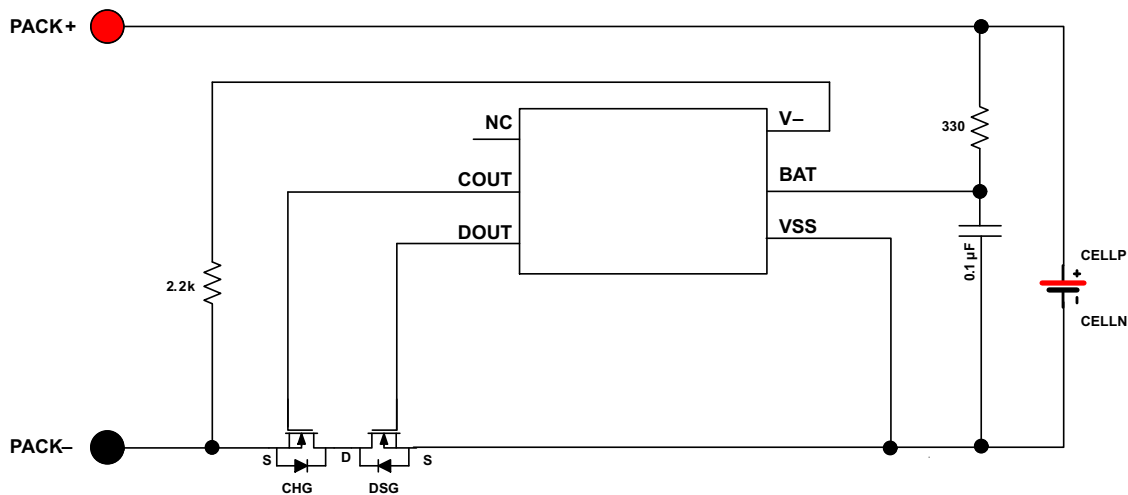
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The bq2970 devices are a family of primary protectors used for protection of the battery pack in the application. The application drives two low-side NMOS FETs that are controlled to provide energy to the system loads or interrupt the power in the event of a fault condition.

10.2 Typical Application



NOTE: The 5-M resistor for an external gate-source is optional.

Figure 26. Typical Application Schematic, bq2970

10.2.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#).

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE at $T_A = 25^\circ\text{C}$
Input voltage range	4.5 V to 7 V
Maximum operating discharge current	7 A
Maximum Charge Current for battery pack	4.5 A
Overvoltage Protection (OVP)	4.275 V
Overvoltage detection delay timer	1.2 s
Overvoltage Protection (OVP) release voltage	4.175 V
Undervoltage Protection (UVP)	2.8 V
Undervoltage detection delay timer	150 ms
Undervoltage Protection (UVP) release voltage	2.9 V
Charge Overcurrent detection (OCC) voltage	-70 mV
Charge Overcurrent Detection (OCC) delay timer	9 ms
Discharge Overcurrent Detection (OCD) voltage	100 mV
Discharge Overcurrent Detection (OCD) delay timer	18 ms

Typical Application (continued)

Table 2. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE at T _A = 25°C
Load Short Circuit Detection (SCC) voltage, BAT to –V ≤ threshold	500 mV
Load Short Circuit Detection (SCC) delay timer	250 μs
Load Short Circuit release voltage, BAT to –V ≥ Threshold	1 V

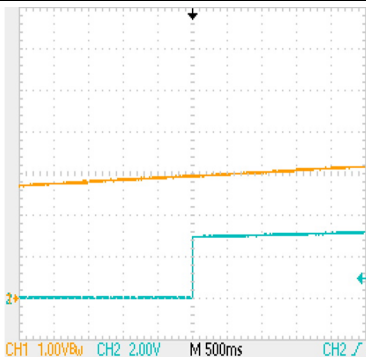
10.2.2 Detailed Design Procedure

NOTE

The external FET selection is important to ensure the battery pack protection is sufficient and complies to the requirements of the system.

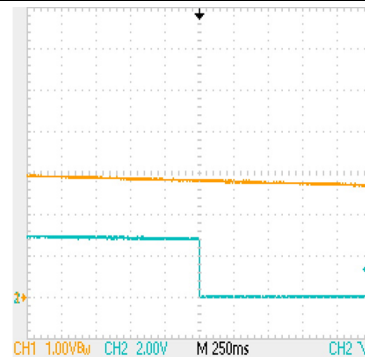
- FET Selection: Because the maximum desired discharge current is 7 A, ensure that the Discharge Overcurrent circuit does *not* trigger until the discharge current is above this value.
- The total resistance tolerated across the two external FETs (CHG + DSG) should be 100 mV/7 A = 14.3 mΩ.
- Based on the information of the total ON resistance of the two switches, determine what would be the Charge Overcurrent Detection threshold, 14.3 mΩ × 4.5 A = 65 mV. Selecting a device with a 70-mV trigger threshold for Charge Overcurrent trigger is acceptable.
- The total R_{ds ON} should factor in any worst-case parameter based on the FET ON resistance, de-rating due to temperature effects and minimum required operation, and the associated gate drive (V_{gs}). Therefore, the FET choice should meet the following criteria:
 - V_{dss} = 25 V
 - Each FET R_{ds ON} = 7.5 mΩ at T_j = 25°C and V_{gs} = 3.5 V
- I_{max} > 50 A to allow for short Circuit Current condition for 350 μs (max delay timer). The only limiting factor during this condition is Pack Voltage/(Cell Resistance + (2 × FET_R_{dsON}) + Trace Resistance).
- Use the CSD16406Q3 FET for the application.
- An RC filter is required on the BAT for noise, and enables the device to operate during sharp negative transients. The 330-Ω resistor also limits the current during a reverse connection on the system.
- TI recommends placing a high impedance 5-MΩ across the gate source of each external FET to deplete any charge on the gate-source capacitance.

10.2.3 Application Performance Plots



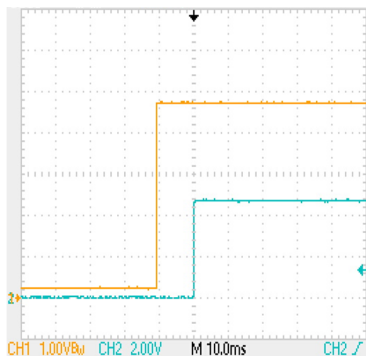
Orange Line (Channel 1) = Power Up Ramp on BAT Pin
 Turquoise Line (Channel 2) = DOUT Gate Drive Output
 DOUT goes from low to high when UVP Recovery = UVP Set Threshold +100 mV

Figure 27. UVP Recovery



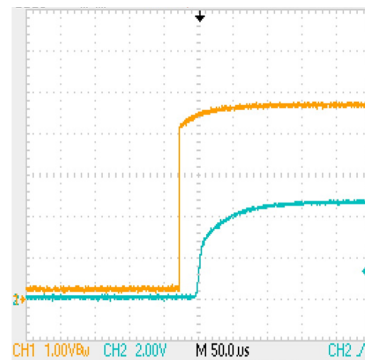
Orange Line (Channel 1) = Power Down Ramp on BAT Pin
 Turquoise Line (Channel 2) = DOUT Gate Drive Output
 DOUT goes from high to low when UVP threshold = UVP set Threshold + set delay time

Figure 28. UVP Set Condition



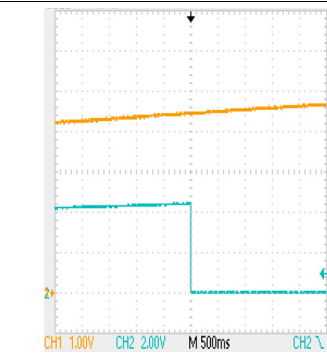
Orange Line (Channel 1) = Power Up Ramp on BAT pin
 Turquoise Line (Channel 2) = DOUT Gate Drive Output

Figure 29. Initial Power Up, DOUT



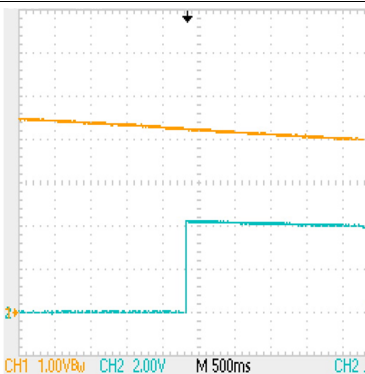
Orange Line (Channel 1) = Power Up Ramp on BAT Pin
 Turquoise Line (Channel 2) = COUT Gate Drive Output

Figure 30. Initial Power Up, COUT



Orange Line (Channel 1) = Power Up Ramp on BAT Pin
 Turquoise Line (Channel 2) = COUT Gate Drive Output
 COUT goes from high to low when OVP threshold = OVP set Threshold + set delay time

Figure 31. OVP Set Condition



Orange Line (Channel 1) = Decrease Voltage on BAT Pin
 Turquoise Line (Channel 2) = COUT Gate Drive Output
 COUT goes from low to high when OVP Recovery = OVP Set Threshold -100 mV

Figure 32. OVP Recovery Condition

11 Power Supply Recommendations

The recommended power supply for this device is a maximum 8-V operation on the BAT input pin.

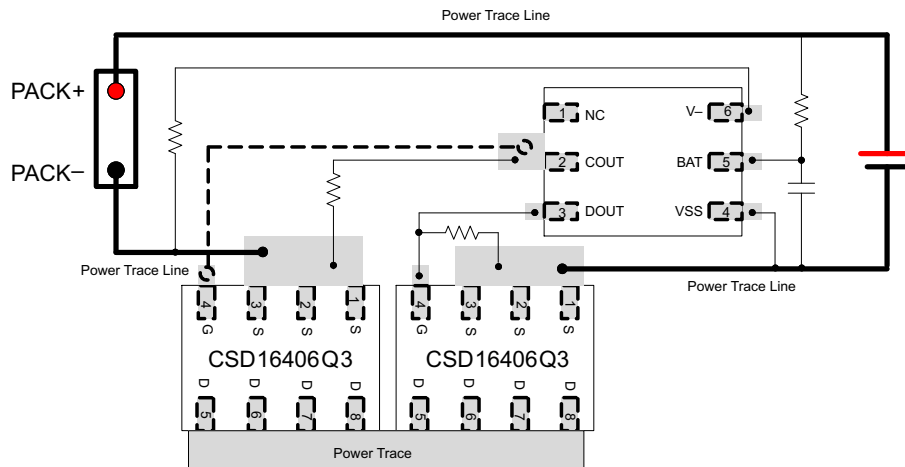
12 Layout

12.1 Layout Guidelines

The following are the recommended layout guidelines:

1. Ensure the external power FETs are adequately compensated for heat dissipation with sufficient thermal heat spreader based on worst-case power delivery.
2. The connection between the two external power FETs should be very close to ensure there is not an additional drop for fault sensing.
3. The input RC filter on the BAT pin should be close to the terminal of the IC.

12.2 Layout Example



○ Via connects between two layers

Figure 33. bq2970 Board Layout

13 器件和文档支持

13.1 相关文档

《[bq29700 单节锂离子电池保护器 EVM 用户指南](#)》 ([SLUUAZ3](#))

13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 3. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
bq2970	单击此处	单击此处	单击此处	单击此处	单击此处
bq2971	单击此处	单击此处	单击此处	单击此处	单击此处
bq2972	单击此处	单击此处	单击此处	单击此处	单击此处
bq2973	单击此处	单击此处	单击此处	单击此处	单击此处

13.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

TI E2E™ 在线社区 [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

13.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 术语表

[SLYZ022](#) — *TI* 术语表。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查看左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29700DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA	Samples
BQ29700DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA	Samples
BQ29701DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FY	Samples
BQ29701DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FY	Samples
BQ29702DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FZ	Samples
BQ29702DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FZ	Samples
BQ29703DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F1	Samples
BQ29703DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F1	Samples
BQ29704DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F2	Samples
BQ29704DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F2	Samples
BQ29705DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3	Samples
BQ29705DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3	Samples
BQ29706DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4	Samples
BQ29706DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4	Samples
BQ29707DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F5	Samples
BQ29707DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F5	Samples
BQ29716DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3P	Samples
BQ29716DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3P	Samples
BQ29717DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3Q	Samples
BQ29717DSET	ACTIVE	WSON	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ29718DSER	ACTIVE	WSO	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3R	Samples
BQ29718DSET	ACTIVE	WSO	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3R	Samples
BQ29723DSER	ACTIVE	WSO	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3S	Samples
BQ29723DSET	ACTIVE	WSO	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3S	Samples
BQ29729DSER	ACTIVE	WSO	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3T	Samples
BQ29729DSET	ACTIVE	WSO	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3T	Samples
BQ29732DSER	ACTIVE	WSO	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3U	Samples
BQ29732DSET	ACTIVE	WSO	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3U	Samples
BQ29733DSER	ACTIVE	WSO	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4Q	Samples
BQ29733DSET	ACTIVE	WSO	DSE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4Q	Samples
BQ29739DSER	PREVIEW	WSO	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KB	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

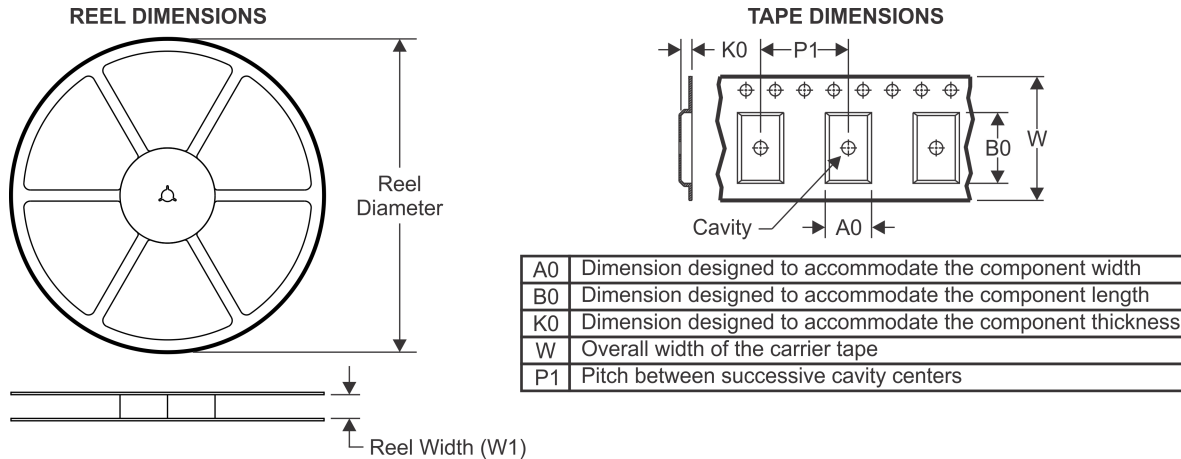
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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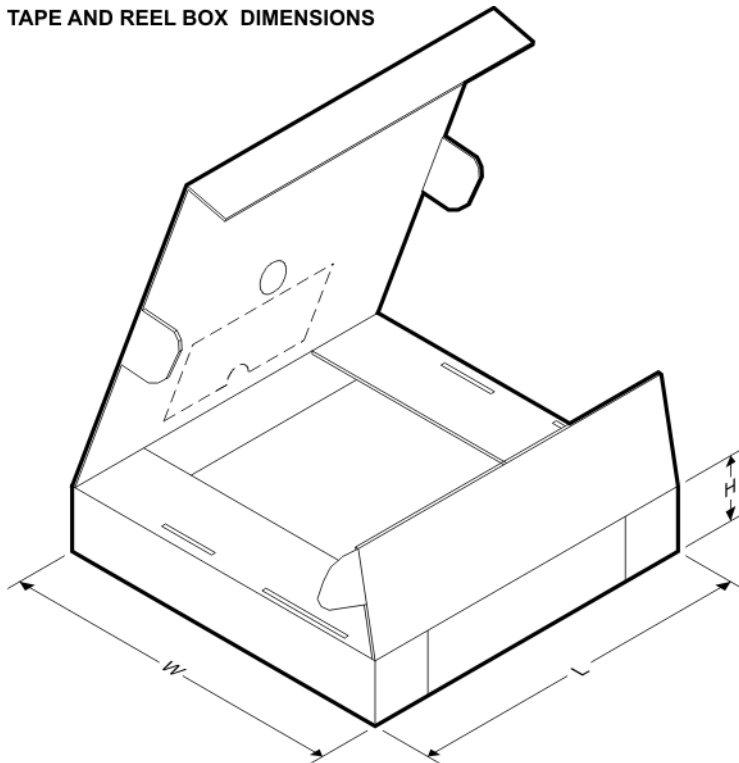
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29700DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29700DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29701DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29701DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29702DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29702DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29703DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29703DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29704DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29704DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29705DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29705DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29706DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29706DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29707DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29707DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29716DSER	WSO	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29716DSET	WSO	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29717DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29717DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29718DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29718DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29723DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29723DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29729DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29729DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29732DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29732DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29733DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
BQ29733DSET	WSON	DSE	6	250	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



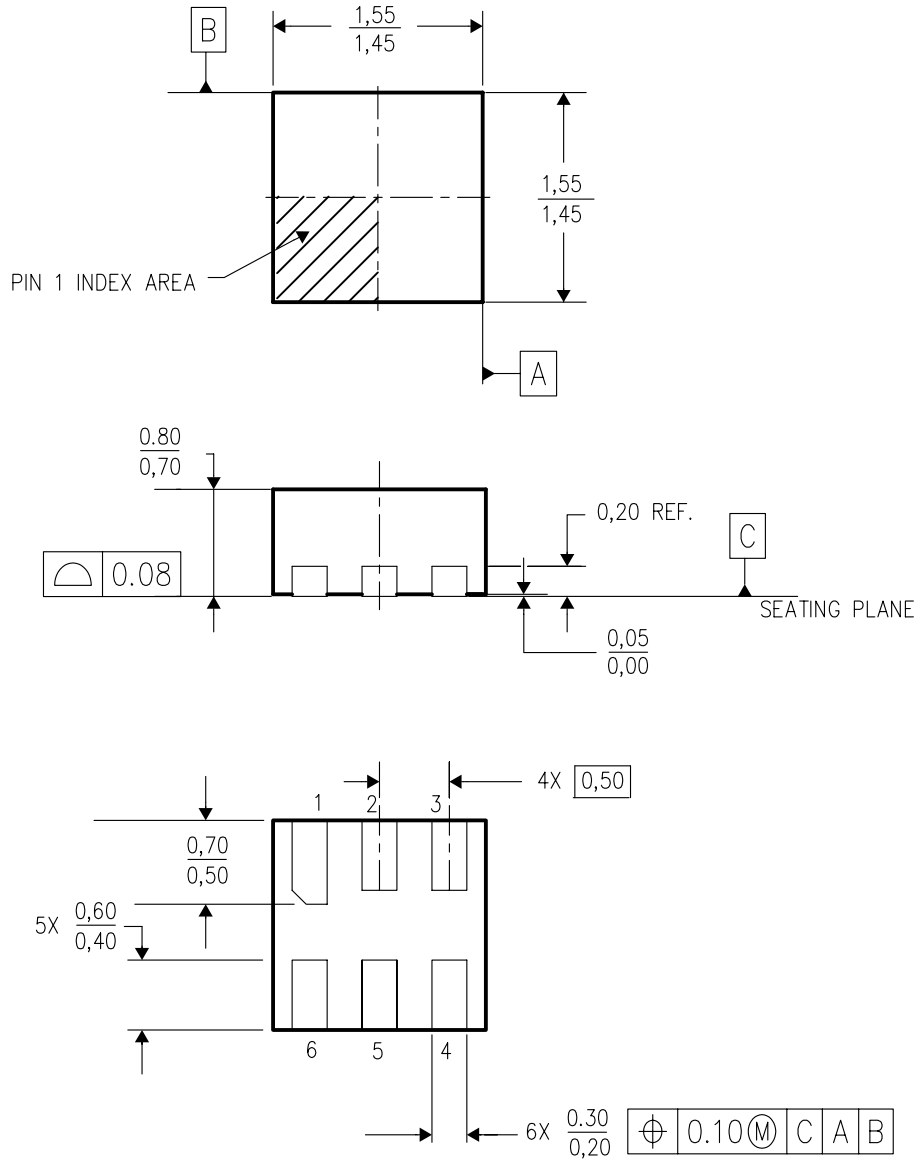
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29700DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29700DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29701DSER	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29701DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29702DSER	WSON	DSE	6	3000	182.0	182.0	20.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29702DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29703DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29703DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29704DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29704DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29705DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29705DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29706DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29706DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29707DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29707DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29716DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29716DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29717DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29717DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29718DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29718DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29723DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29723DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29729DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29729DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29732DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29732DSET	WSON	DSE	6	250	182.0	182.0	20.0
BQ29733DSE	WSON	DSE	6	3000	182.0	182.0	20.0
BQ29733DSET	WSON	DSE	6	250	182.0	182.0	20.0

DSE (S-PDSO-N6)

PLASTIC SMALL OUTLINE

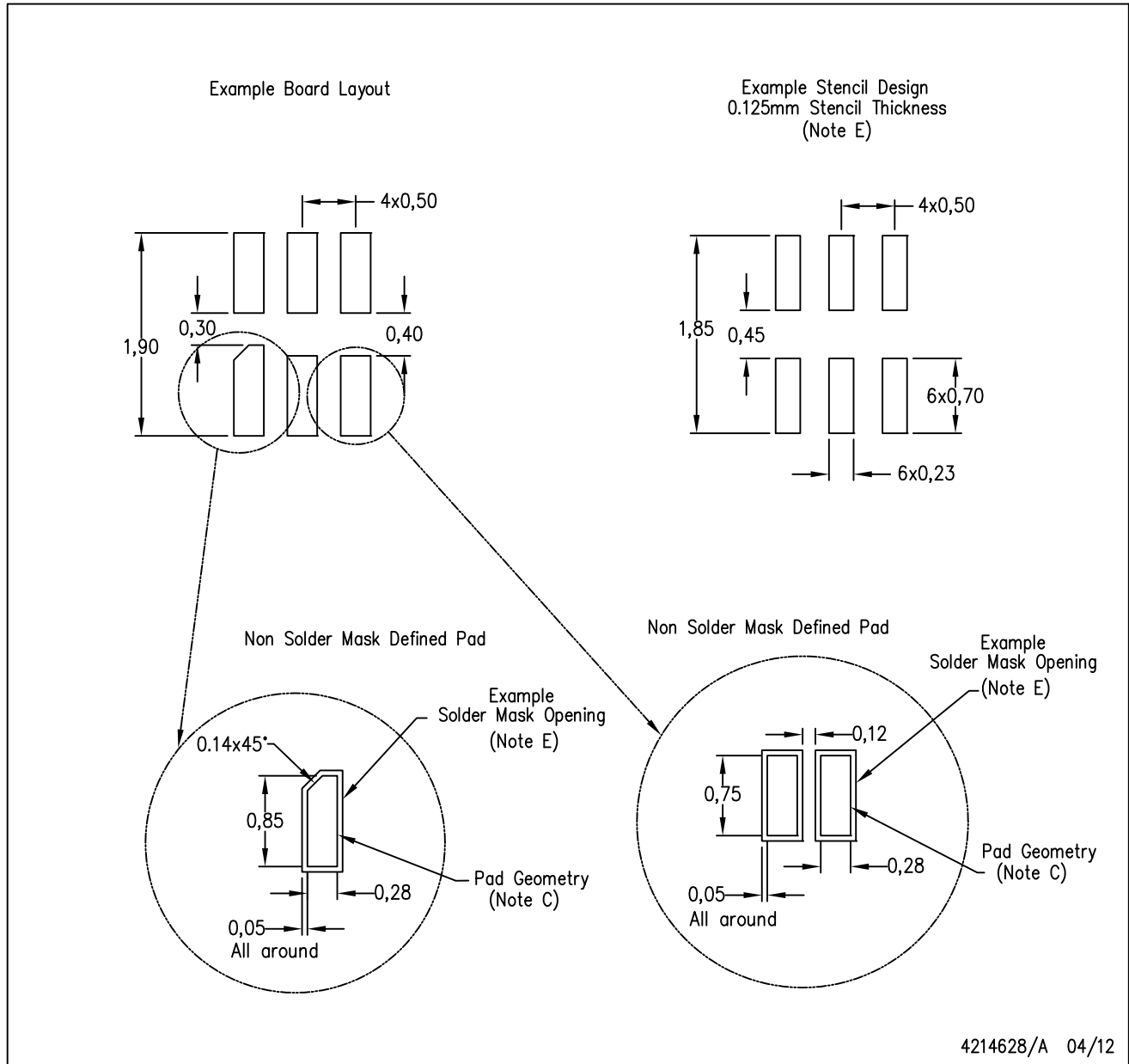


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- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - D. This package is lead-free.

DSE (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for solder mask tolerances.

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