UCC2751x 单通道高速低侧栅极驱动器（基于 CMOS 输入阈值并具有峰值为 4A 的拉/灌电流驱动能力）

1 特性

- 低成本栅极驱动器，是 NPN 和 PNP 分立解决方案的优质替代产品
- 与 TI 的 TPS2828 和 TPS2829 器件引脚兼容
- 4A 峰值拉电流和 4A 峰值灌电流对称驱动
- 快速传播延迟（典型值 17ns）
- 快速上升和下降时间（典型值 8ns 和 7ns）
- 4.5V 至 18V 单电源范围
- VDD 欠压闭锁 (UVLO) 期间输出保持低电平（确保加电和断电时无毛刺脉冲运行）
- CMOS 输入逻辑阈值（带滞后的电源电压的函数）
- 实现高抗噪性的滞后逻辑阈值
- 实现使能功能的 EN 引脚（可不连接）
- 当输入引脚悬空时输出保持在低电平
- 输入引脚绝对最大电压电平不受 VDD 引脚偏置电源电压的限制
- -40°C 至 140°C 的运行温度范围
- 5 引脚 DBV 封装（小外形尺寸晶体管封装 (SOT)-23）

2 应用

- 开关模式电源
- 直流-直流转换器
- 用于数字电源控制器的伴随栅极驱动器器件
- 太阳能、电机控制、不间断电源 (UPS)
- 用于新上市的宽带隙电源器件（例如 GaN）的栅极驱动器

3 说明

UCC27518 和 UCC27519 单通道高速低侧栅极驱动器器件可有效驱动金属氧化物半导体场效应晶体管 (MOSFET) 和绝缘栅双极型晶体管 (IGBT) 电源开关。UCC27518 和 UCC27519 采用的设计方案可最大程度减少击穿电流，从而为电容负载提供较高的峰值拉/灌电流脉冲，同时提供轨到轨驱动能力以及超短的传播延迟（典型值为 17ns）。

当 VDD = 12V 时，UCC27518 和 UCC27519 可提供峰值为 4A 的灌/拉（对称驱动）电流驱动能力。

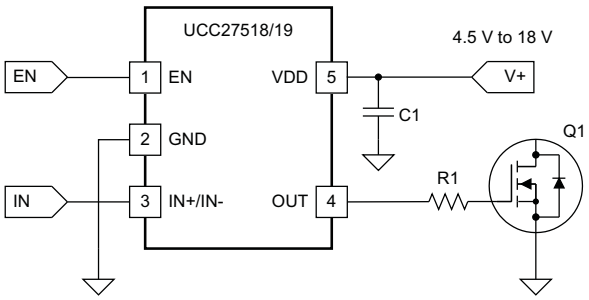
UCC27518 和 UCC27519 具有 4.5V 至 18V 的宽 VDD 范围，以及 –40°C 至 140°C 的宽温度范围。 当超出 VDD 工作范围时，VDD 引脚上的内部欠压闭锁 (UVLO) 电路可使输出保持低电平。 该器件不仅能够工作在低于 5V 的低电压下，还具备同类产品中最佳的开关特性，因此非常适用于驱动诸如 GaN 功率半导体器件等新上市的宽带隙电源开关器件。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC27518	SOT-23 (5)	2.90mm x 1.60mm
UCC27519		

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



目录

4 修订历史记录

Changes from Original (May 2012) to Revision A **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

5 说明（续）

UCC27518 和 UCC27519 的输入引脚阈值基于 CMOS 逻辑电路，其中阈值电压是 VDD 电源电压的函数。 输入阈值上限典型值 (V_{IN-H}) 是 V_{DD}的 55%，而输入阈值下限典型值 (V_{IN-L}) 是 V_{DD} 的 39%。 阈值上下限之间的宽滞后（通常为 V_{DD}的 16%）提供了出色的抗噪性，并且使用户能够通过在输入脉宽调制 (PWM) 信号与器件的 INx 引脚之间使用 RC 电路来引入延迟。

UCC27518 和 UCC27519 的 EN 引脚上还特有一个可悬空的使能功能。 将 EN 引脚置于未连接状态，可分别实现 UCC27518，UCC27519 与 TPS2828，TPS2829 之间的引脚兼容性。 EN 引脚的电压阈值是固定的，不会随 V_{DD} 引脚偏置电压变化。 使能阈值上限典型值 (V_{EN-H}) 为 2.1V，而使能阈值下限典型值 (V_{EN-L}) 为 1.25V。

6 Device Comparison Table

The UCC2751x family of gate driver products (Table 1) represent TI's latest generation of single-channel, low-side high-speed gate driver devices featuring high-source/sink current capability, industry best-in-class switching characteristics and a host of other features (Table 2) all of which combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

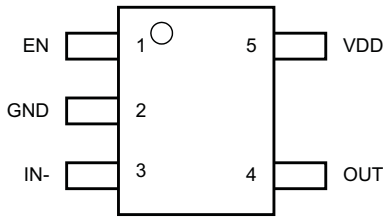
Table 1. UCC2751x Product Family Summary

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE/SINK)	INPUT THRESHOLD LOGIC
UCC27511DBV(1)	SOT-23, 6 pin	4-A/8-A (Asymmetrical Drive)	CMOS/TTL-Compatible (low voltage, independent of VDD bias voltage)
UCC27512DRS(1)	3 mm x 3 mm WSON, 6 pin		
UCC27516DRS(1)	3 mm x 3 mm WSON, 6 pin	4-A/4-A (Symmetrical Drive)	
UCC27517DBV(1)	SOT-23, 5 pin		
UCC27518DBV	SOT-23, 5 pin		CMOS (follows VDD bias voltage)
UCC27519DBV	SOT-23, 5 pin		

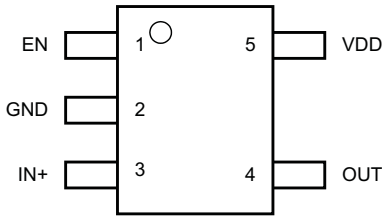
(1) Visit www.ti.com for the latest product datasheet.

7 Pin Configuration and Functions

UCC27518
SOT-23 DBV
(Top View)



UCC27519
SOT-23 DBV
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	EN	I	Enable input: (EN biased LOW disables output regardless of Input state, EN biased high or floating enables output, EN is allowed to float hence it is pin-to-pin compatible with TPS282X N/C pin)
2	GND	—	Ground: All signals referenced to this pin
3	IN–	I	Input: Inverting input in the UCC27518, output held LOW if IN– is unbiased or floating
	IN+	I	Input: Noninverting input in the UCC27519, output held LOW if IN+ is unbiased or floating
4	OUT	O	Sourcing and sinking current output of driver
5	VDD	I	Supply input

8 Specifications

8.1 Absolute Maximum Ratings(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	20	V
OUT voltage		–0.3	VDD + 0.3	
Output continuous current	I_{OUT_DC} (source/sink)		0.3	A
Output pulsed current (0.5 µs)	I_{OUT_pulsed}(source/sink)		4	
IN+, IN-(4), EN		–0.3	20	V
Operating virtual junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	
	Reflow		260	
Storage temperature, T_{stg}		–65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the data sheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(4) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	–40		140	°C
Input voltage, (IN+ and IN–) and Enable (EN)	0		18	V

8.4 Thermal Information

THERMAL METRIC		UCC27518 SOT-23 DBV 5 PINS	UCC27519 SOT-23 DBV(1) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	217.6	217.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance(1)	85.8	85.8	
$R_{\theta JB}$	Junction-to-board thermal resistance(1)	44.0	44.0	
ψ_{JT}	Junction-to-top characterization parameter(1)	4.0	4.0	
ψ_{JB}	Junction-to-board characterization parameter(1)	43.2	43.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

VDD = 12 V, $T_A = T_J$ = -40 °C to 140 °C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BIAS CURRENTS							
$I_{DD(off)}$	Startup current	VDD = 3.4 V	IN+ = VDD (UCC27519), IN- = GND (UCC27518)	51	85	123	µA
			IN+ = GND (UCC27519), IN- = VDD (UCC27518)	51	70	103	
UNDERVOLTAGE LOCKOUT (UVLO)							
V_{ON}	Supply start threshold	T_A = 25 °C		3.85	4.20	4.57	V
		T_A = -40 °C to 140°C		3.80	4.20	4.67	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	
V_{DD_H}	Supply voltage hysteresis			0.19	0.3	0.45	
INPUTS (IN+, IN–)							
V_{IN_H}	Input signal high threshold	VDD = 4.5 V			55	62	%VDD
V_{IN_L}	Input signal low threshold			31	39		
V_{IN_HYS}	Input signal hysteresis				16		
V_{IN_H}	Input signal high threshold	VDD = 12 V			55	59	
V_{IN_L}	Input signal low threshold			31	39		
V_{IN_HYS}	Input signal hysteresis				16		
V_{IN_H}	Input signal high threshold	VDD = 18 V			55	58	
V_{IN_L}	Input signal low threshold			35	38		
V_{IN_HYS}	Input signal hysteresis				17		
ENABLE (EN)							
V_{EN_H}	Enable signal high threshold	VDD = 12 V			2.1	2.3	V
V_{EN_L}	Enable signal low threshold			1.00	1.25		
V_{EN_HYS}	Enable hysteresis				0.86		
SOURCE/SINK CURRENT							
$I_{SRC/SNK}$	Source/sink peak current(1)	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz			-4/+4		A
OUTPUTS (OUT)							
V_{DD}-V_{OH}	High output voltage	VDD = 12 V I_{OUT} = -10 mA			50	90	mV
		VDD = 4.5 V I_{OUT} = -10 mA			60	130	
V_{OL}	Low output voltage	VDD = 12 I_{OUT} = 10 mA			5	11	
		VDD = 4.5 V I_{OUT} = 10 mA			6	12	
R_{OH}	Output pullup resistance(2)	VDD = 12 V I_{OUT} = -10 mA			5.0	7.5	Ω
		VDD = 4.5 V I_{OUT} = -10 mA			5.0	11.0	
R_{OL}	Output pulldown resistance	VDD = 12 V I_{OUT} = 10 mA			0.5	1.0	
		VDD = 4.5 V I_{OUT} = 10 mA			0.6	1.2	

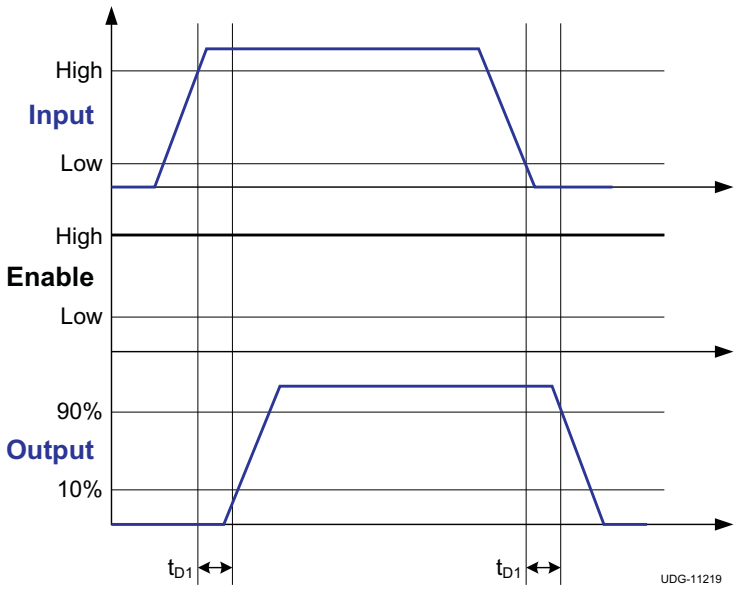
(1) Ensured by Design.
(2) R_{OH} represents on-resistance of P-Channel MOSFET in pullup structure of the UCC27518 and UCC27519's output stage.

8.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

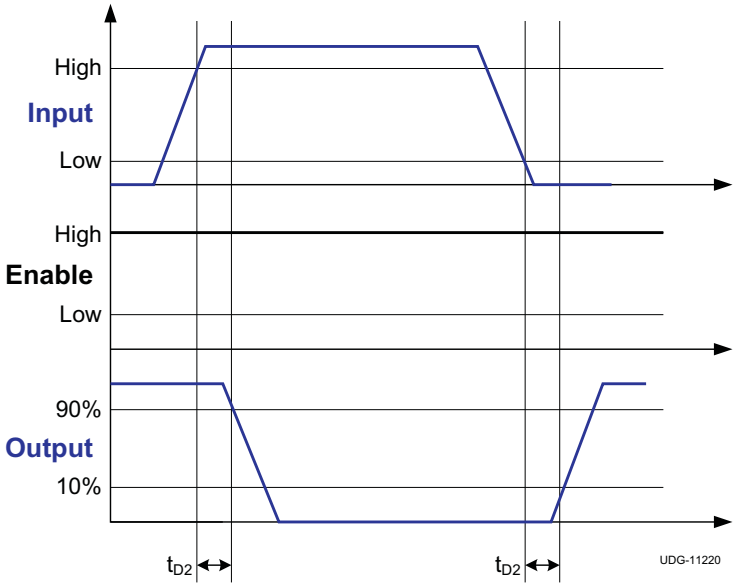
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time(1)	C_{LOAD} = 1.8 nF		8	12	ns
t_F	Fall time(1)	C_{LOAD} = 1.8 nF		7	11	
t_{D1}	IN+ to output propagation delay(1)	VDD = 10 V 7-V input pulse, C_{LOAD} = 1.8 nF	6	17	25	
t_{D2}	IN- to output propagation delay(1)	VDD = 10 V 7-V input pulse, C_{LOAD} = 1.8 nF	6	17	24	
t_{D3}	EN to output high propagation delay(1)	C_{LOAD} = 1.8 nF, 5-V enable pulse	4	12	16	
t_{D4}	EN to output low propagation delay(1)	C_{LOAD} = 1.8 nF, 5-V enable pulse	4	12	19	

(1) See timing diagrams in Figure 1, Figure 2, Figure 3, and Figure 4.



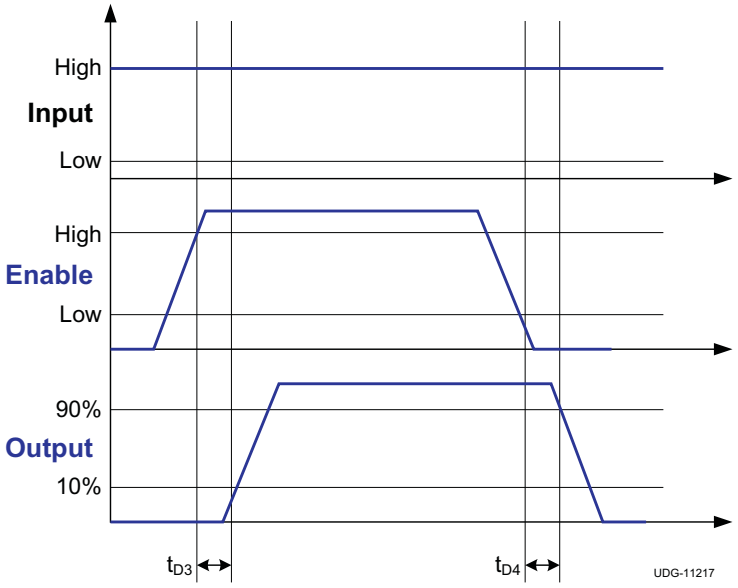
(In+ Pin, UCC27519)

Figure 1. Noninverting Configuration



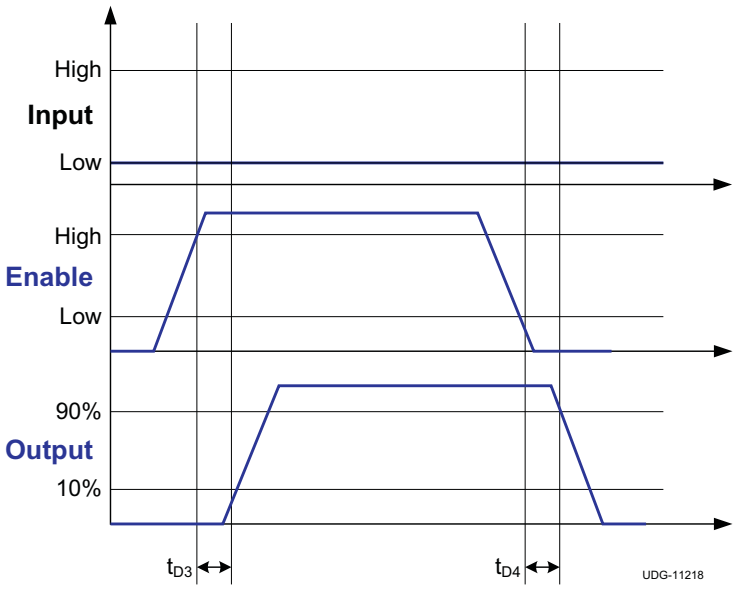
(In– Pin, UCC27518)

Figure 2. Inverting Configuration



(Noninverting Configuration, UCC27519)

Figure 3. Enable and Disable Function



(Inverting Configuration, UCC27518)

Figure 4. Enable and Disable Function

8.7 Typical Characteristics

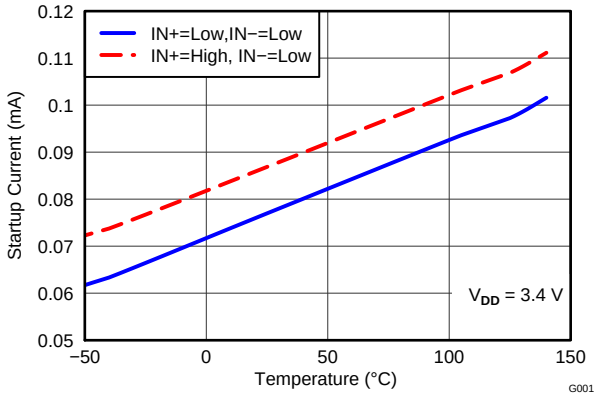


Figure 5. Start-Up Current vs Temperature

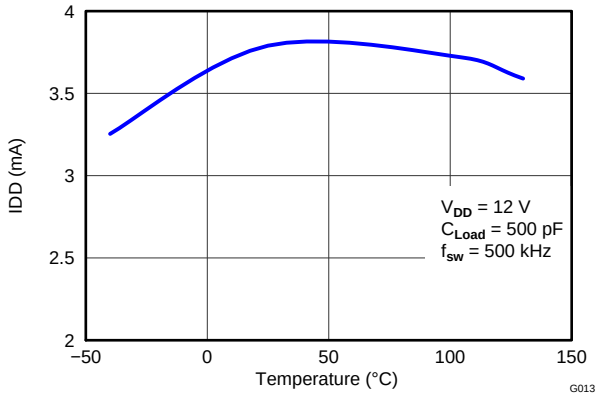


Figure 6. Operating Supply Current vs Temperature (Output Switching)

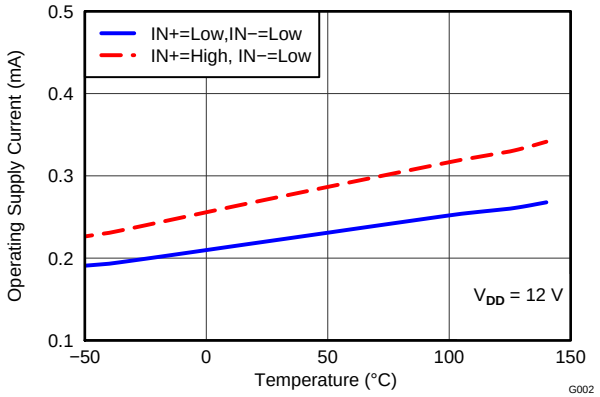


Figure 7. Supply Current vs Temperature (Output In DC On/Off Condition)

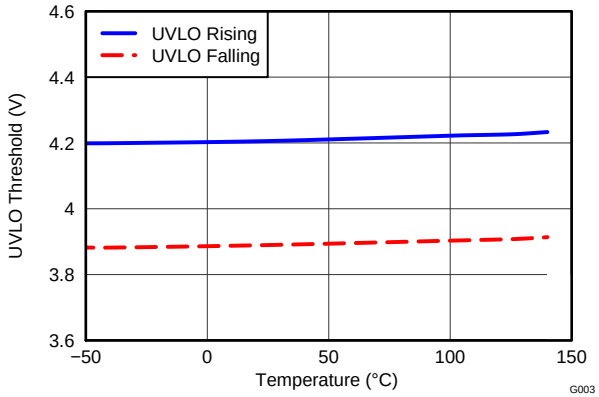


Figure 8. UVLO Threshold Voltage vs Temperature

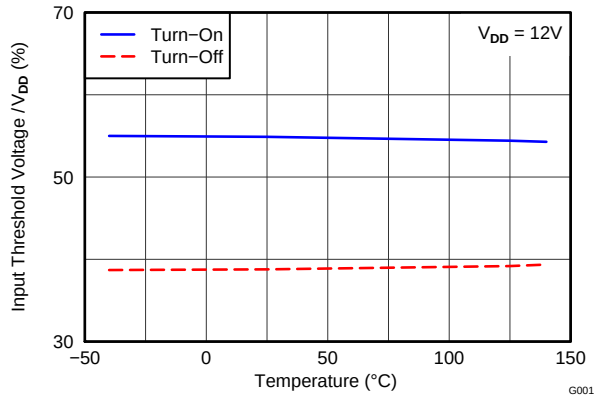


Figure 9. Input Threshold vs Temperature

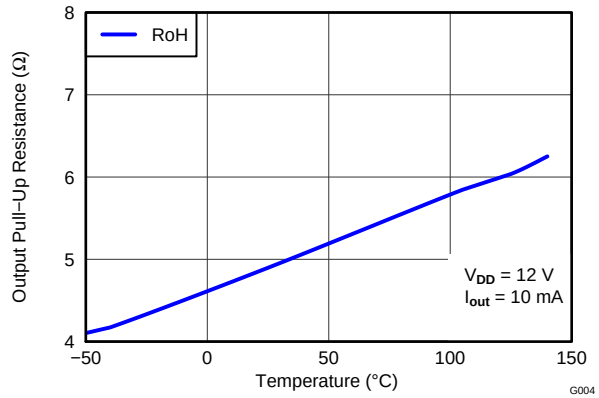


Figure 10. Output Pullup Resistance vs Temperature

Typical Characteristics (continued)

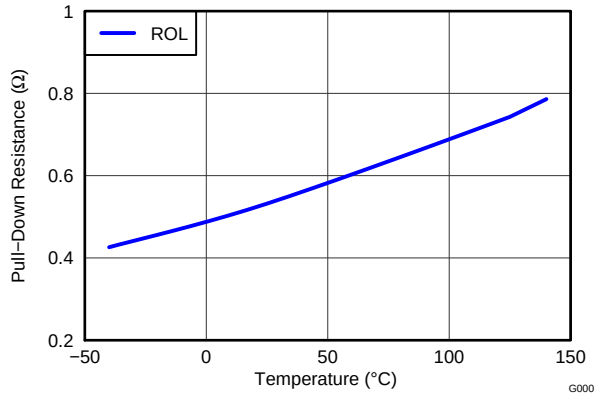


Figure 11. Output Pulldown Resistance vs Temperature

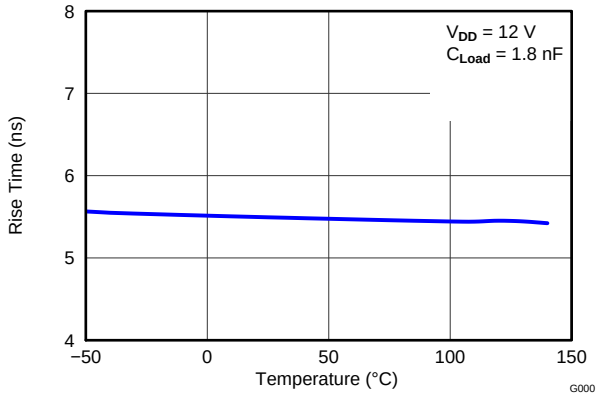


Figure 12. Rise Time vs Temperature

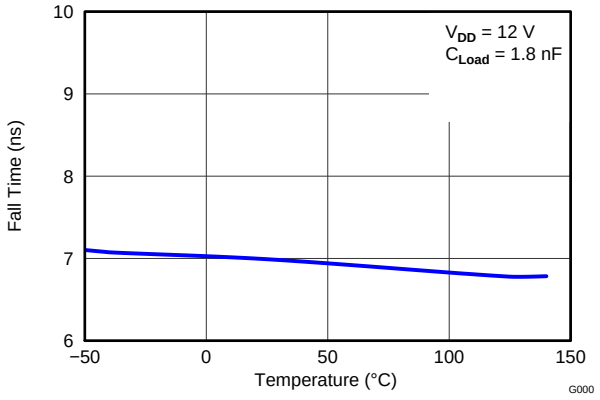


Figure 13. Fall Time vs Temperature

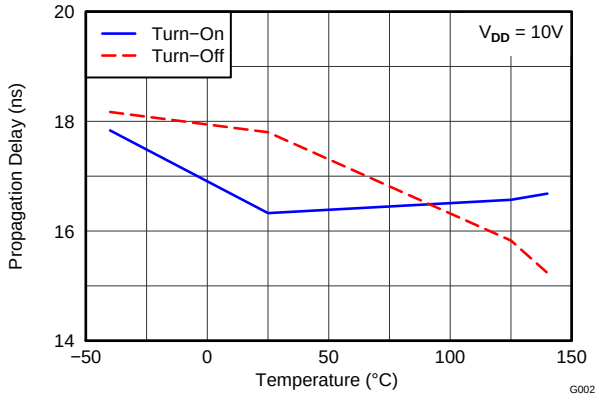


Figure 14. Input To Output Propagation Delay vs Temperature

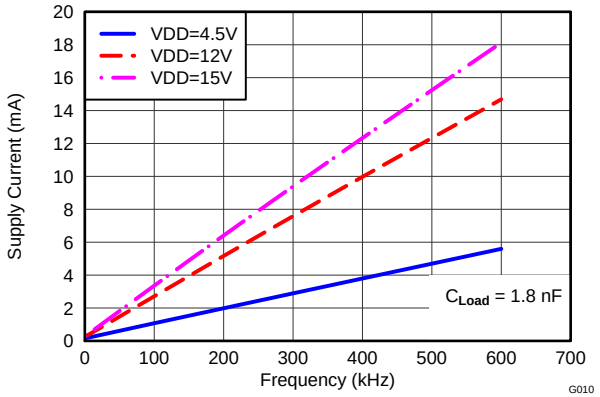


Figure 15. Operating Supply Current vs Frequency

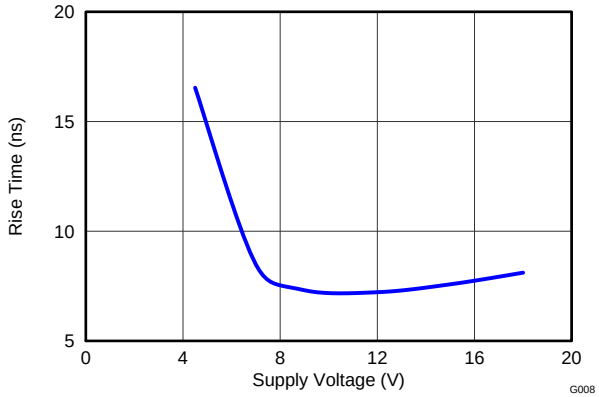


Figure 16. Rise Time vs Supply Voltage

Typical Characteristics (continued)

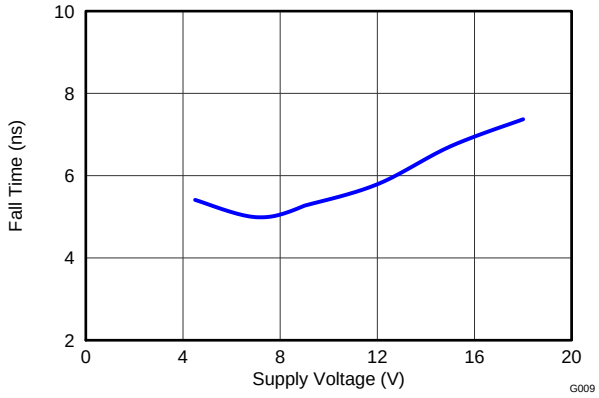


Figure 17. Fall Time vs Supply Voltage

9 Detailed Description

9.1 Overview

The UCC2751x single-channel, high-speed, low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC2751x device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to- rail drive capability and extremely small propagation delay of 13 ns (typical).

The UCC2751x device provides 4-A source, 4-A sink (symmetrical drive) peak-drive current capability. The device is designed to operate over a wide V_{DD} range of 4.5 to 18 V, and a wide temperature range of -40°C to 140°C. Internal undervoltage lockout (UVLO) circuitry on the V_{DD} pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging wide band-gap power-switching devices such as GaN power-semiconductor devices.

The UCC27518 device follows an inverting logic between the input and output, while the UCC27519 device follows noninverting logic. The input pins of the devices are based on what is known as CMOS input threshold logic. In CMOS input logic, the threshold voltage level is a function of the bias voltage on the V_{DD} pin of the device. This offers the benefits of higher noise immunity due to the higher threshold voltage (compared to logic level input thresholds), as well as the ability to accept slow dV/dt input signals for manipulating the propagation delay between the PWM controller signal and the gate driver output. For system robustness, internal pull-up and pull-down resistors on the input pins ensure that outputs are held low when the input pins are in floating condition.

Table 2. UCC2751x Family of Features and Benefits

FEATURE	BENEFIT
High Source/Sink Current Capability 4 A/8 A (Asymmetrical) – UCC27511/2 4 A/4 A (Symmetrical) – UCC27516/7	High current capability offers flexibility in employing UCC2751x family of devices to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low pulse transmission distortion
Expanded VDD Operating range of 4.5 V to 18 V	Flexibility in system design Low VDD operation ensures compatibility with emerging wide band-gap power devices such as GaN
Expanded Operating Temperature range of -40 °C to 140 °C (See Electrical Characteristics table)	
VDD UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down
Outputs held low when input pins (INx) in floating condition	Safety feature, especially useful in passing abnormal condition tests during safety certification
Ability of input pins (and enable pin in UCC2751x) to handle voltage levels not restricted by VDD pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
Split output structure in UCC27511 (OUTH, OUTL)	Allows independent optimization of turnon and turnoff speeds
Strong sink current (8 A) and low pull-down impedance (0.375 Ω) in UCC27511/2	High immunity to C x dV/dt Miller turnon events
CMOS/TTL compatible input threshold logic with wide hysteresis in UCC27511/2/6/7	Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power
CMOS input threshold logic in UCC2751x (VIN_H – 70% VDD, VIN_L – 30% VDD)	Well suited for slow input voltage signals, with flexibility to program delay circuits (RCD)

9.2 Functional Block Diagrams

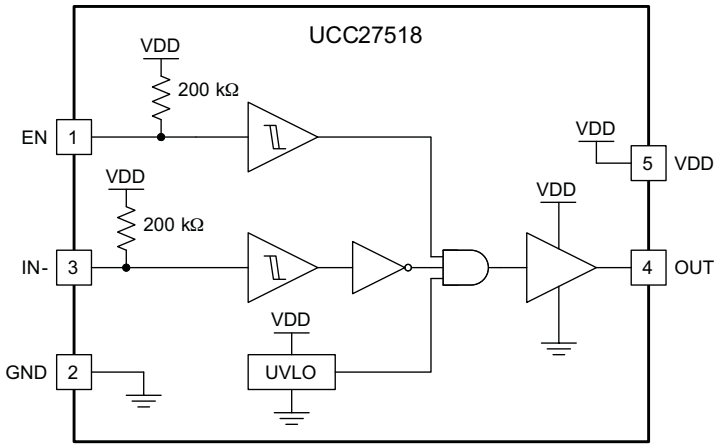


Figure 18. UCC27518 Functional Block Diagram

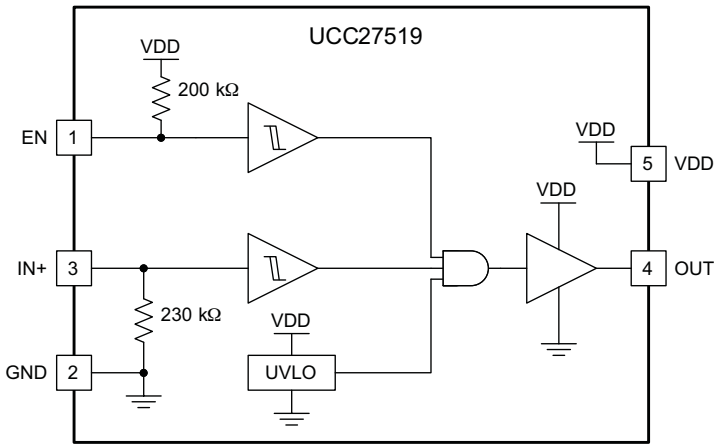


Figure 19. UCC27519 Functional Block Diagram

9.3 Feature Description

9.3.1 VDD and Undervoltage Lockout

The UCC2751x devices have internal Under Voltage LockOut (UVLO) protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition (i.e. when V_{DD} voltage less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide bandgap power semiconductor devices.

For example, at power up, the UCC2751x driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the noninverting device (PWM signal applied to IN+ pin) shown below, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. In the inverting device (PWM signal applied to IN- pin) shown below the output remains LOW until the UVLO threshold is reached, and then the output is out-phase with the input.

Feature Description (continued)

Since the driver draws current from the VDD pin to bias all internal circuits, for the best high-speed circuit performance, two VDD bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the VDD to GND pins of the gate driver. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

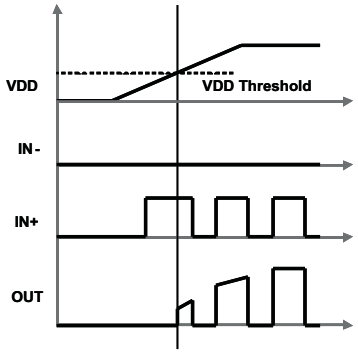


Figure 20. Power-Up (Noninverting Drive)

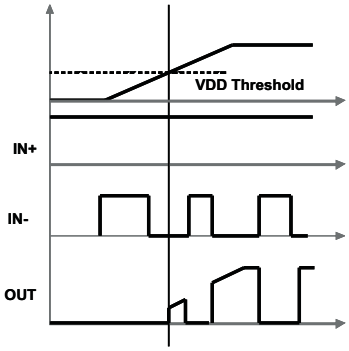


Figure 21. Power-Up (Inverting Drive)

9.3.2 Operating Supply Current

The UCC27518 and UCC27519 features very low quiescent I_{DD} currents. The typical operating supply current in Under Voltage LockOut (UVLO) state and fully-on state (under static and switching conditions) are summarized in Figure 5, Figure 6 and Figure 7. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer Figure 7) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to switching and finally any current related to pull-up resistors on the unused input pin. For example when the inverting input pin is pulled low additional current is drawn from VDD supply through the pull-up resistors (refer to *Pin Configuration and Functions* for the device Block Diagram). Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the IDD current as a function of switching frequency at different VDD bias voltages under 1.8-nF switching load is provided in Figure 15. The strikingly linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to its high-speed characteristics.

9.3.3 Input Stage

The input pins of UCC27518 and UCC27519 are based on CMOS input logic where the threshold voltage level is a function of the bias voltage applied on the VDD pin. Typically, the Input High Threshold (V_INH) is 55% VDD and Input Low Threshold (VIN_L) is 39% VDD. Hysteresis (typically 19% VDD) available on the input threshold offers noise immunity. With high VDD voltages resulting in wide hysteresis, slow dV/dt input signals are acceptable in the INx pins and RC circuits can be inserted between the input PWM signal and the INx pins of UCC2751x, to program a delay between the input signal and output transition.

9.3.4 Enable Function

The Enable pin is based on a noninverting configuration (active high operation). When EN pin is driven high the output is enabled and when EN pin is driven low the output is disabled. Unlike input pin, the enable pin threshold is based on a TTL/CMOS compatible input threshold logic that does not vary with the supply voltage. Typically, the Enable High Threshold (V_ENH) is 2.1 V and Enable Low Threshold (VEN_L) is 1.25 V. Thus the EN pin can be effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The EN pin is internally pulled up to VDD using pull-up resistor as a result of which the output of the device is enabled in the default state. Hence the EN pin can be left floating or Not Connected (N/C) for standard operation, when enable feature is not needed. Essentially, this allows the UCC27518/19 devices to be pin-to-pin compatible with TI's previous generation drivers TPS2828/9 respectively, where pins #1 is N/C pin.

Feature Description (continued)

9.3.5 Output Stage

The UCC27518 and UCC27519 are capable of delivering 4-A source, 4-A sink (symmetrical drive) at VDD = 12 V. The output stage of the UCC27518 and UCC27519 devices are illustrated in Figure 22. The UCC27518 and UCC27519 devices features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turnon transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device is able to deliver a brief boost in the peak-sourcing current enabling fast turn on.

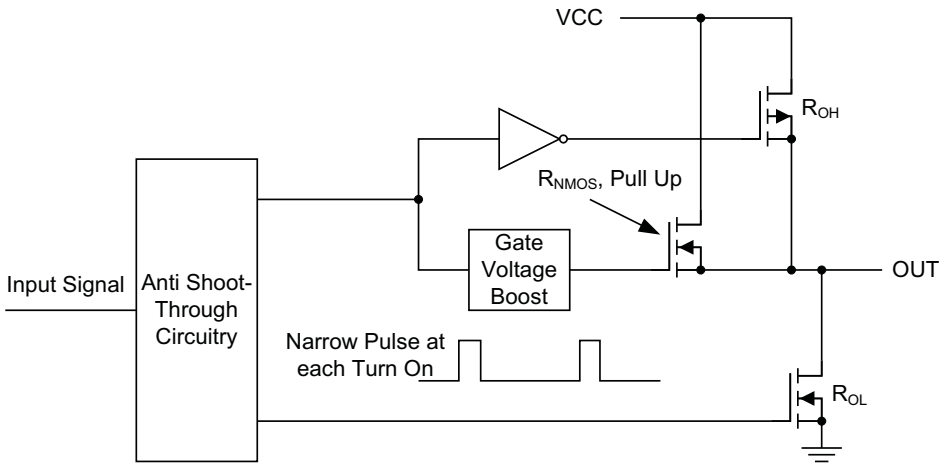


Figure 22. UCC2751x Gate Driver Output Structure

The R_{OH} parameter (see *Electrical Characteristics*) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by R_{OH} parameter. The pull-down structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see *Electrical Characteristics*), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC27518 and UCC27519, the effective resistance of the hybrid pull-up structure is approximately 1.4 x R_{OL}.

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

9.3.6 Low Propagation Delays

The UCC27518 and UCC27519 driver device features best-in-class input-to-output propagation delay of 17 ns (typ) at VDD = 12 V. This promises the lowest level of pulse transmission distortion available from industry standard gate driver devices for high-frequency switching applications. As seen in Figure 14, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

9.4 Device Functional Modes

Table 3. Device Logic Table

EN	UCC27518		UCC27519	
	IN– PIN	OUT PIN	IN+ PIN	OUT PIN
H	L	H	L	L
H	H	L	H	H
L	Any	L	Any	L
Any	x(1)	L	x(1)	L
x(1)	L	H	L	L
x(1)	H	L	H	H

(1) x = Floating Condition

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers and the gates of the power semiconductor devices. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself. Finally, emerging wide band-gap power device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate drive capability. These requirements include operation at low VDD voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

10.2 Typical Application

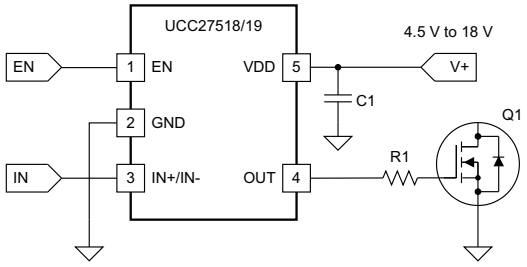


Figure 23. Typical Application Diagram

10.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type.

Table 4. Design Parameters

Design Parameter	Example Value
Input-to-Output Logic	Noninverting
Input Threshold Type	CMOS type
VDD Bias Supply Voltage	10 V (Minimum), 13 V (Nominal), 15 V (Peak)
Peak Source and Sink Currents	Minimum 3 A Source, Minimum 3 A Sink
Enable and Disable Function	Yes, Needed
Propagation Delay	Maximum 40 ns or less

10.2.2 Detailed Design Procedure

10.2.2.1 Input-to-Output Logic

The design must specify which type of input-to-output configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then the noninverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, the inverting configuration must be chosen. The UCC27518 and UCC27519 devices follow inverting and noninverting logic, respectively.

10.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller used with the gate driver device. The UCC27518 and UCC27519 devices feature CMOS input threshold logic, with wide hysteresis. In CMOS input threshold logic, the threshold voltage level is a function of the bias voltage on the V_{DD} pin of the device. The typical high threshold is 55% of V_{DD} supply voltage, and the typical low threshold is 39% of V_{DD} supply voltage at V_{DD}=12V. There is built-in hysteresis, which is typically 16% of V_{DD} supply voltage. See *Electrical Characteristics* for the actual input threshold voltage levels and hysteresis specifications for the UCC27518 and UCC27519 devices at different V_{DD} bias levels.

In most applications, the absolute value of the threshold voltage offered by the CMOS logic will be higher (eg.VINH = 5.5 V if V_{DD} = 10 V) than what is offered by logic level threshold devices. This offers the following benefits:

- Better noise immunity due to the higher threshold level desirable in high power systems.
- Ability to accept slow dV/dt input signals, which allows designers to use RCD circuits on the input pin to program propagation delays in the application, as shown in Figure 24.

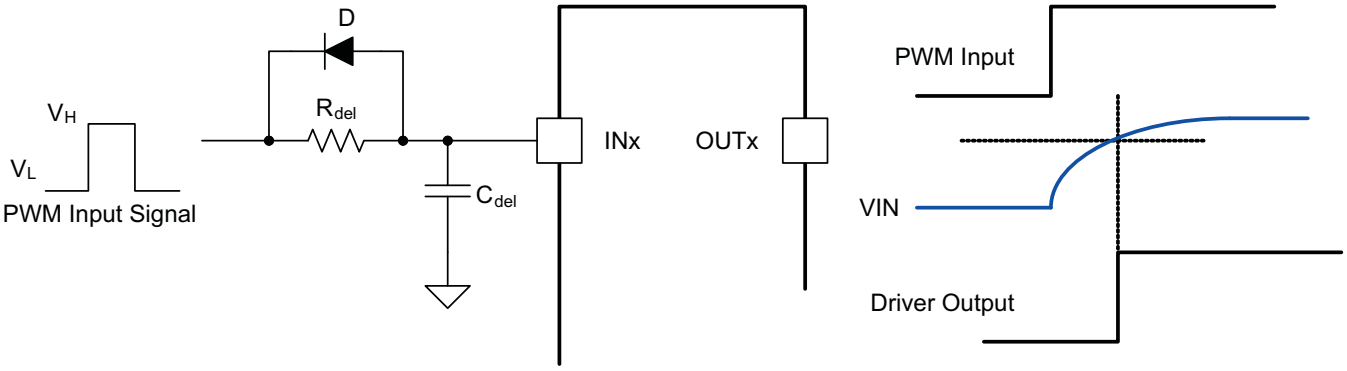


Figure 24. Using RCD Circuits

$$t_{del} = -R_{del}C_{del} \times \ln\left(\frac{V_L - V_{IN\_H}}{V_H - V_L} + 1\right) \quad (1)$$

As a result of the CMOS input logic, the UCC27518 and UCC27519 devices cannot be driven directly by logic level control signals from microcontrollers, digital power controllers, or DSPs. The UCC27518 and UCC27519 are ideally suited for being driven by analog controllers driven by the same V_{DD} voltage as the gate driver devices.

10.2.2.3 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pin of the device should never exceed the values listed in *Recommended Operating Conditions*. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turn on and turnoff. With certain power switches, a positive gate voltage may be required for turn on, and a negative gate voltage may be required for turnoff, in which case the V_{DD} bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC27518 and UCC27519 devices can be used to drive a variety of power switches, such as Si MOSFETs (for example, VGS = 4.5 V, 10 V, 12 V), IGBTs (VGE = 15 V, 18 V), and wide-band gap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

10.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turn on and turnoff should be as fast as possible, to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET. Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dVDS/dt).

For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV_{DS}/dt of 20V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive, hard-switching application, and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in on state) must be completed in approximately 20 ns or less.

When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to the power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(TH)}$. To achieve the targeted dV_{DS}/dt, the gate driver must be capable of providing the QGD charge in 20 ns or less. In other words, a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC27518 and UCC27519 gate driver is capable of providing 4-A peak sourcing current, which exceeds the design requirement and has the capability to meet the necessary switching speed.

The 2.4x overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET, along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver.

To illustrate this, consider the output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle ($\frac{1}{2} \times I_{PEAK} \times$ time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the dI/dt, the full peak current capability of the gate driver may not be fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I_{PEAK} value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, place the gate driver device very close to the power MOSFET and design a tight gate drive-loop with minimal PCB trace inductance to realize the full peak-current capability of the gate driver.

10.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. The UCC27518 and UCC27519 devices offer the Enable pin, which achieves this.

10.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used, and the acceptable level of pulse distortion to the system. The UCC27518 and UCC27519 devices feature industry best-in-class 17-ns (typical) propagation delays, which ensure very little pulse distortion and allow operation at very high-frequencies. See *Switching Characteristics* for the propagation and switching characteristics of the UCC27518 and UCC27519 devices.

10.2.3 Application Curve

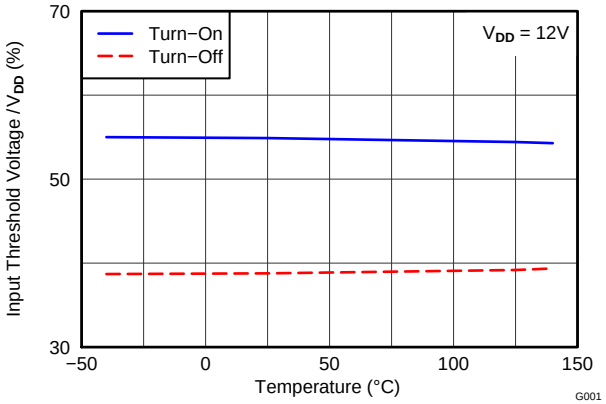


Figure 25. Input Threshold vs Temperature

11 Power Supply Recommendations

The bias supply voltage range for which the UCC27518 and UCC27519 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition with the V_{DD} pin voltage below the $V_{(ON)}$ supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. When the V_{DD} pin bias voltage has exceeded the threshold voltage and the device begins to operate, if the voltage drops, the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. While operating at or near the 4.5 V range, ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device to avoid triggering device shutdown.

During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup the device does not begin operation until the V_{DD} pin voltage has exceeded above the $V_{(ON)}$ threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. The charge for source current pulses delivered by the OUT pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the V_{DD} pin. Therefore, ensure that local bypass capacitors are provided between the V_{DD} and GND pins and located as close to the device as possible, for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. TI recommends to have 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device, and another surface-mount capacitor of few microfarads added in parallel.

12 Layout

12.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current, fast-switching circuit to provide appropriate device operation and design robustness. The UCC27518 and UCC27519 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak-current capability is even higher (4-A/4-A peak current is at VDD = 12 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. TI highly recommends using low-inductance SMD components such as chip resistors and chip capacitors.
- The turnon and turnoff current loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances – during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition

Layout Guidelines (continued)

to noise shielding, the ground plane can help in power dissipation as well.

12.2 Layout Example

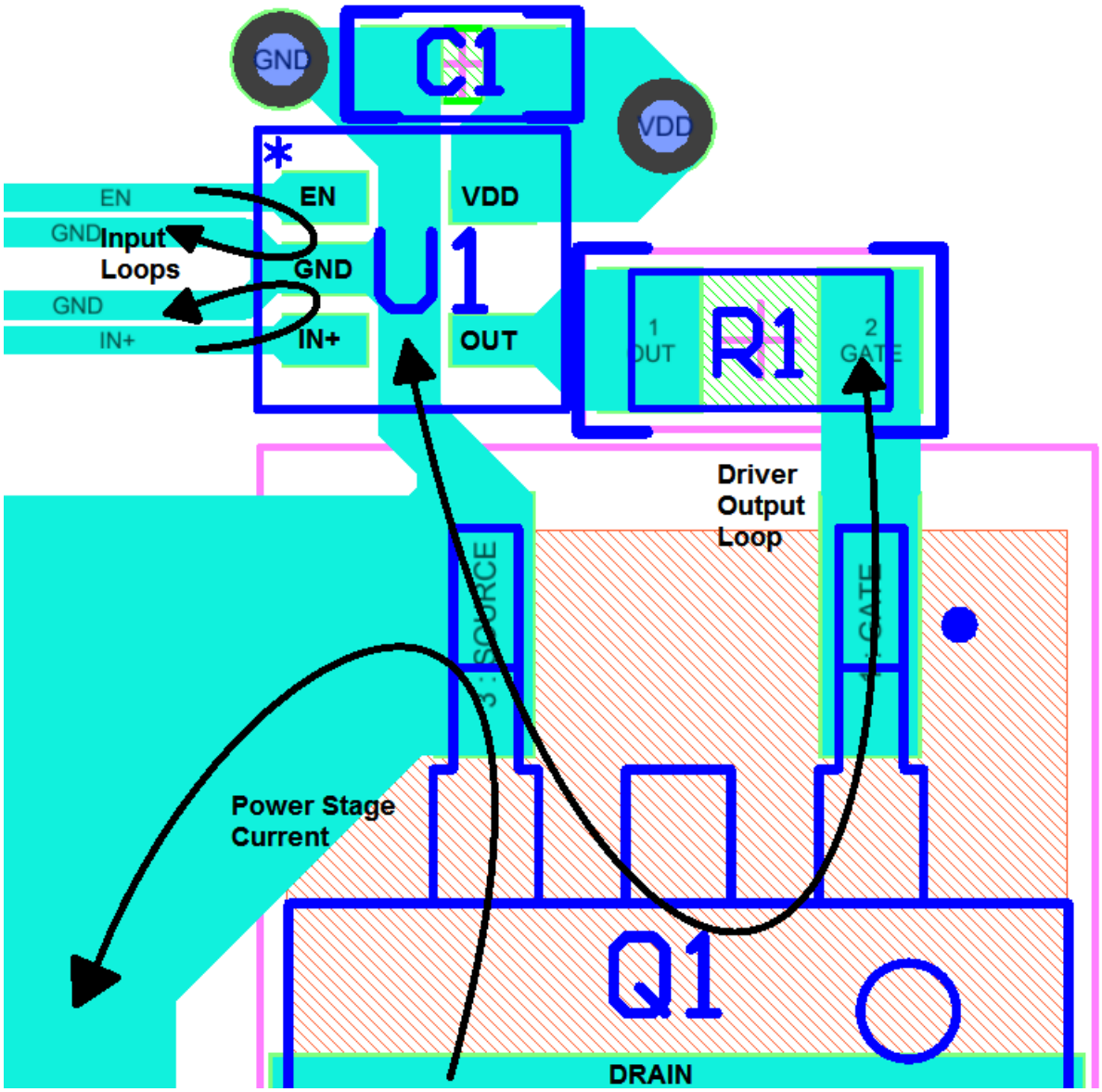


Figure 26. Layout Example

12.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. For a gate driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in *Thermal Information*. For detailed information regarding the thermal information table, refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (SPRA953).

12.4 Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \quad (2)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through etc). The UCC27518 and UCC27519 features very low quiescent currents (less than 1 mA, refer Figure 7) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out).
- Switching frequency.
- Use of external gate resistors.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver (3)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW}$$

where

- f_{SW} is the switching frequency (4)

The switching load presented by a power MOSFET/IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equation, $Q_G = C_{LOAD}$ x V_{DD}, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \quad (5)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = Q_G \times V_{DD} \times f_{SW} \times \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure) = 1.4 x R_{OL} (6)

13 器件和文档支持

13.1 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 5. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
UCC27518	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC27519	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.2 商标

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13.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27518DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7518	Samples
UCC27518DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7518	Samples
UCC27519DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7519	Samples
UCC27519DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7519	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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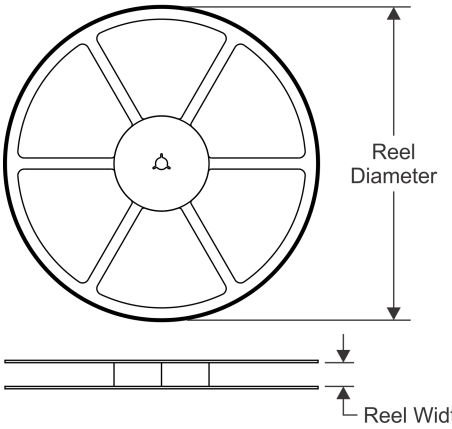
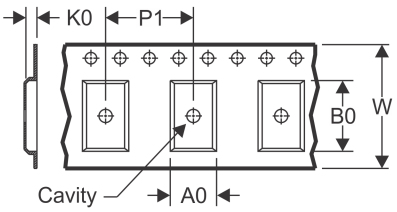
TAPE AND REEL INFORMATION

REEL DIMENSIONS

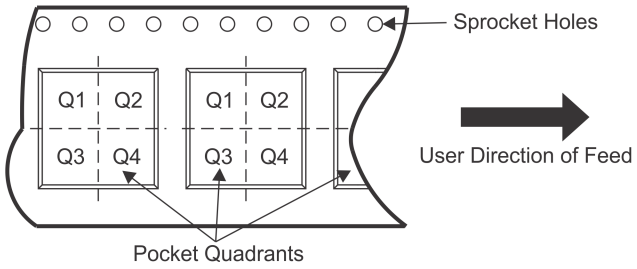


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

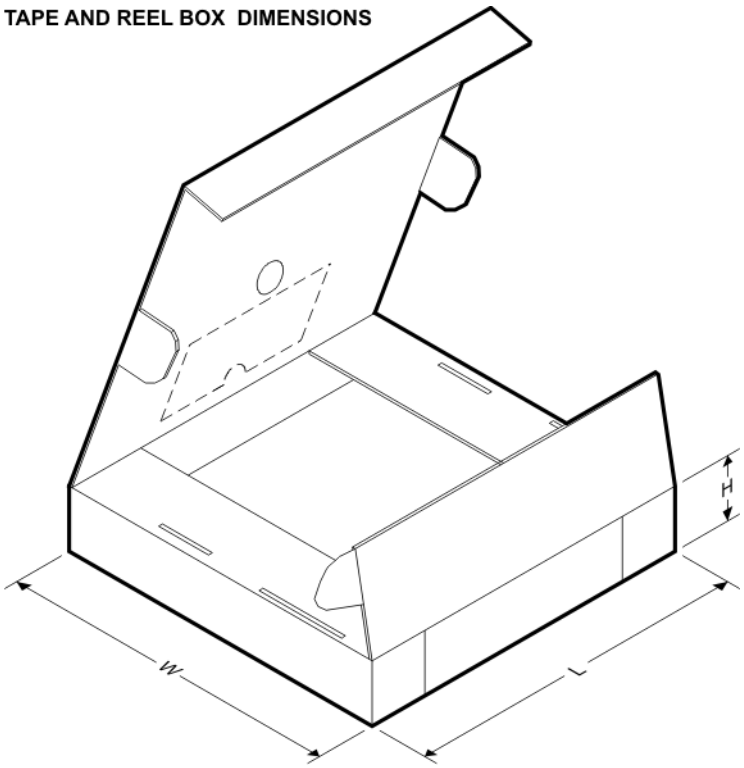
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27518DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27518DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27519DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27519DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

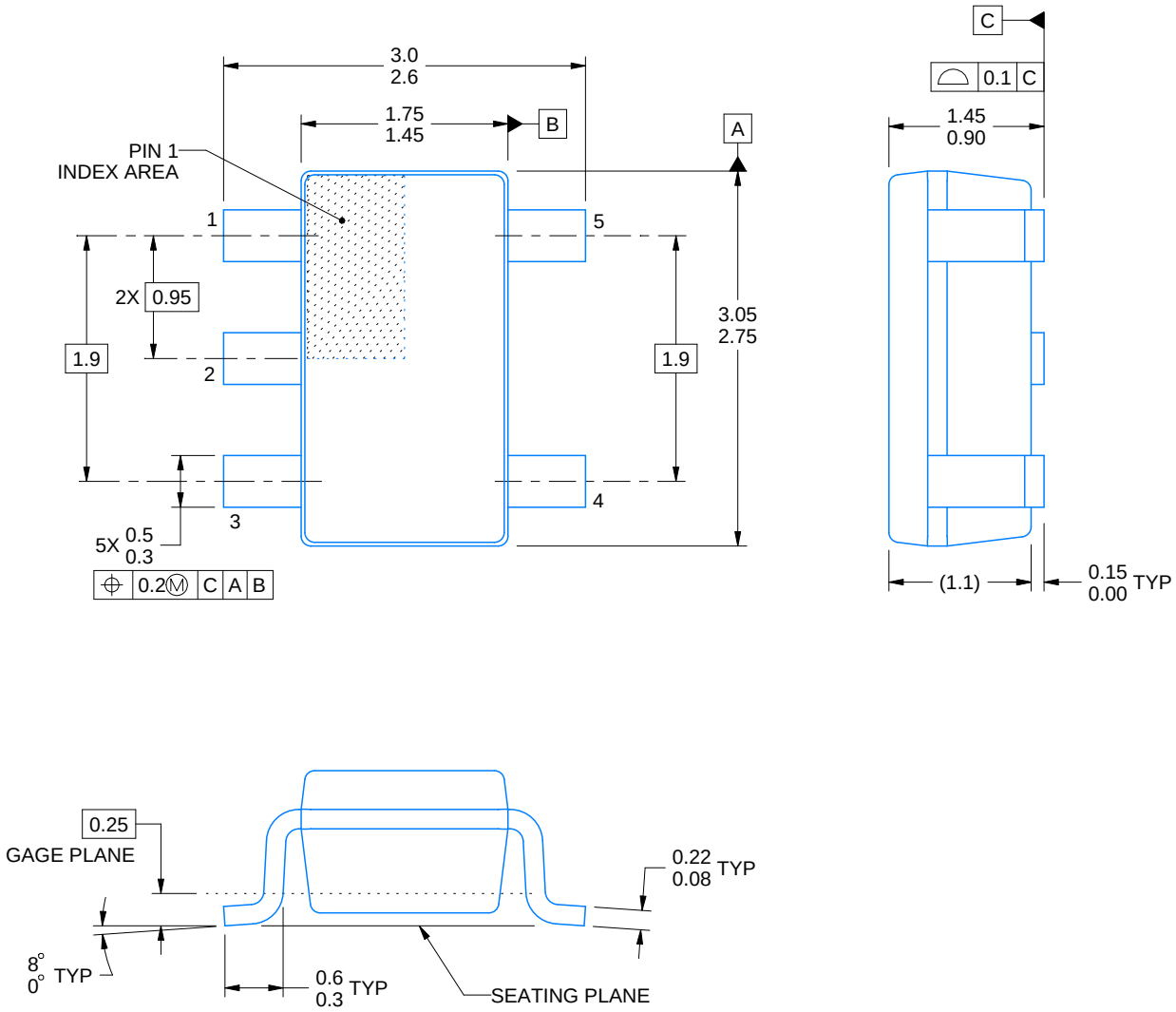
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27518DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
UCC27518DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0
UCC27519DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
UCC27519DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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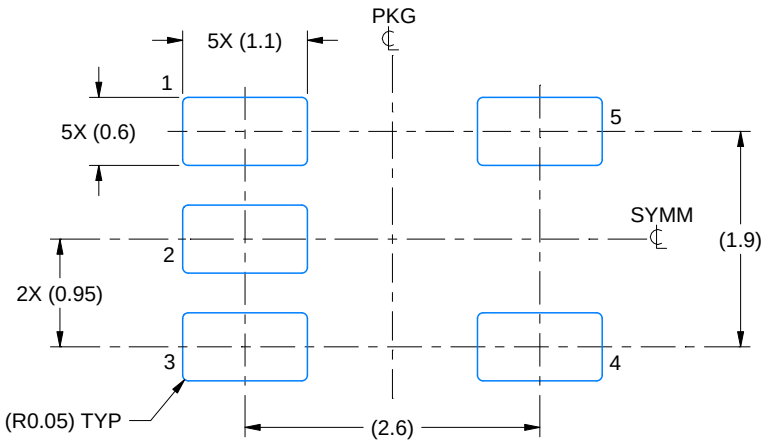
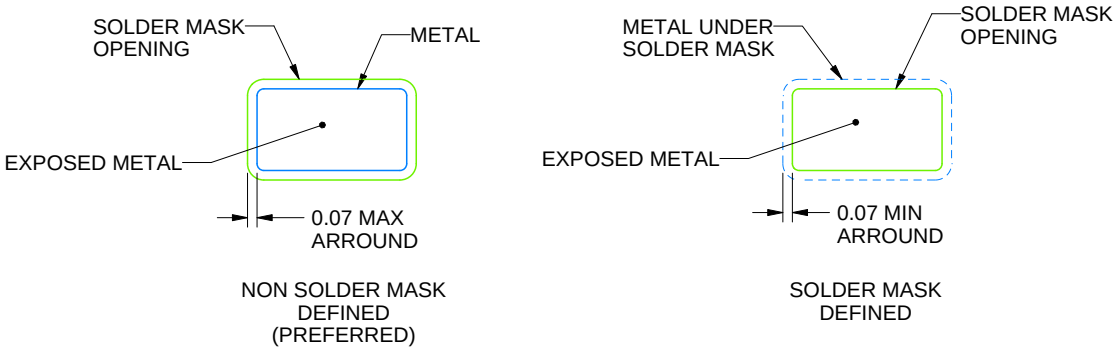
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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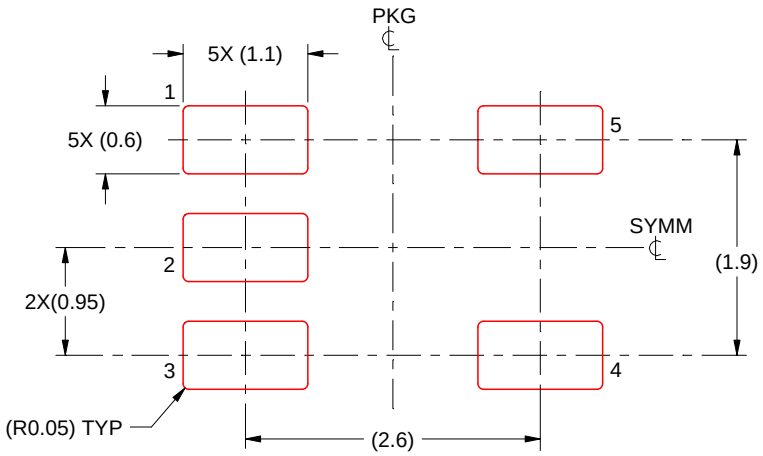
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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