# A Multi-resonant Gate Driver for Very-High-Frequency (VHF) Resonant Converters

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***Abstract*—This paper presents the design and implementation of a Very-High-Frequency (VHF) multi-resonant gate drive circuit. The design procedure is greatly simplified compared with some VHF self-oscillating multi-resonant gate drivers presented in previous works. The proposed circuit has the potential to reduce long start-up time required in a self-oscillating resonant gate drive circuit and to better utilize fast transient capability of VHF converters. A prototype resonant gate driver is demonstrated and able to reduce 60 % of the gate driving loss of a 20 MHz 32 W Class–E power amplifier with Si MOSFET.**

## I. Introduction

A principle method to achieve reduced size and weight, better transient response, and full integration of state-of-art power converters is to increase switching frequencies. During the past three decades, resonant converters [1]–[5] have been successfully demonstrated up to 10s of MHz. Applying RF circuit design techniques to dc-dc power conversion has pushed the switching frequency of power converters using discrete components beyond 100 MHz [6], [7]. As switching frequency further increases, the percentage of gate driving losses among the total power loss can become unacceptable in both hard-switching PWM coverters and resonant converters. In order to reduce the gate driving losses, several resonant gate drive techniques have been proposed [8]–[10] for PWM converters. The common idea is based on using a inductor, which is essentially a current source, to charge/discharge the gate capacitance. Most of previous demonstrations [8]–[10] using discrete devices are below 1 MHz. The experimentally reported total gate energy saving using these techniques are typically less than 50%. The advantages and disadvantages of these resonant gate drive circuits for PWM converters are summarized in [11].

To first principles, conventional gate driving loss can be approximated as $f_s V_g Q_g$, where $f_s$ is the switching frequency, $V_g$ is gate drive supply voltage, $Q_g$ is the total gate charge provided to the main MOSFET. A typical MOSFET $Q_g$ vs $V_g$ waveform assuming a constant charging current is shown in Fig 1. For VHF resonant converters switching at above 10 MHz, the required gate drive power of an advanced Si trench MOSFET can be higher than the total conduction loss. GaN FETs require much smaller $Q_g$ and $V_g$ to operate with than Si MOSFETs. However, due to much smaller package and thermal mass of GaN FETs, even tiny amount of extra loss can increase the junction temperate and so does the conduction loss in main power circuit. Therefore, resonant gate drive is usually necessary in VHF converters. Different from PWM converters,

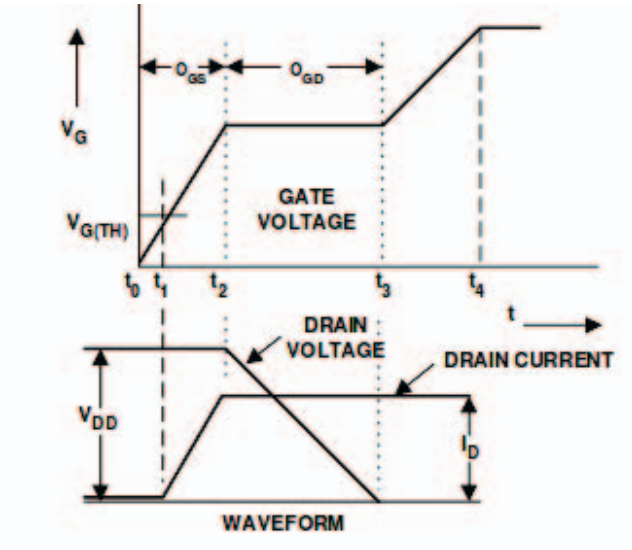


**Fig. 1:** Typical $Q_g$ vs $V_g$ plot

resonant converters are more sensitive to switching frequency but less sensitive to duty cycle variation. The duty ratio of gate driving clock in series/parallel resonant converter and class $E^2$ dc-dc converter is always close to 50% [1], [3], [12]. Due to the sensitiveness to switching frequency and simplicity of integration, the resonant gate drive techniques that have been demonstrated for VHF resonant converters in [6], [7], [12], [13] are based on self-oscillating gate drive topoglogies. Passive phase shift network is added between the drain and gate of a transistor to make an oscillator circuit.

VHF resonant gate drivers driving MOSFET with a sinusoidal $V_{gs}(t)$ [7], [13], [14] are simple to design but at a cost of higher conduction loss in the main power MOSFET due to the slower transition between cut-off region and linear region. [6] demonstrated a 100 MHz self-oscillating multi-resonant gate drive which drives the main power MOSFET with a quasi-square wave $V_{gs}(t)$. The circuit uses a multi-resonant network to synthesize a quasi-square voltage waveform by summation of the $1^{st}$ harmonic component and $3^{rd}$ harmonic component with certain ratio. Effectively, $V_{gs}(t)$ is a trapezoidal wave which has faster rising/falling time than a sine wave. This self-resonant gate drive in [6] was able to recover 90% of the gate energy. However, a problem of this gate driver (oscillator) is that it requires a start-up time to reach steady state. In addition to this start-up time of the gate driver, the main power

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circuit also requires several switching cycles to reach steady state and efficiently delivers power. Therefore, when ON/OFF control is used for regulation, the modulation frequency was limited to around 200 kHz which does not fully utilize the fast transient capability of 100 MHz switching frequency. Moreover, fine tuning necessary in the design of passive phase shift network and multi-resonant impedance makes this self-oscillating resonant gate drive approach really complex.

This paper presents the design of a similar multi-resonant gate driver which drives the main MOSFET with a trapezoidal waveform but not based on self-oscillating topologies presented in [6], [7], [12], [13]. Consequently, the design procedure is greatly simplified and the long start-up time of the self-oscillating gate driver can be eliminated. The proposed gate drive use a conventional half-bridge circuit with a multi-resonant passive network to generate a trapezoidal waveform at the gate of the main MOSFET in a VHF converter. The circuit is shown in Fig. 3. The rest of the paper is organized as follows. The loss in a quasi-square wave gate drive circuit is analyzed in Section II. The design principles of the proposed circuit are presented in Section III. Two Class–E power amplifiers with both conventional gate driver and proposed resonant gate driver circuit are built to prove the concept. The simulation and experimental results of are presented in Section IV. The prototype resonant gate driver can drive a Si trench MOSFET with a 20 MHz trapezoidal $V_{gs}(t)$ and save $60\%$ of the gating power without affecting the main Class–E converter's efficiency. The total efficiency including the gating loss is increased from $81.5\%$ to $84.5\%$ compared with conventional gate driver.

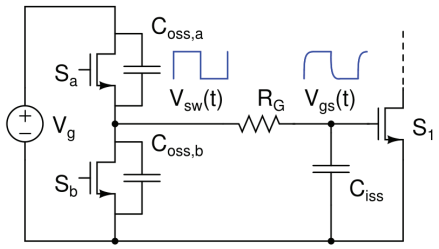



**Fig. 2:** Conventional gate drive

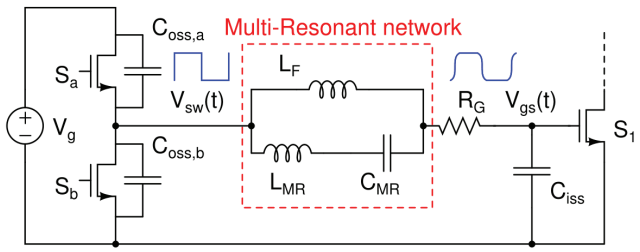



**Fig. 3:** Proposed multi-resonant gate drive

## II. Quasi-square Wave Gate Driving Loss

A conventional gate drive circuit is shown in Fig. 2. Typically, it consists of a half-bridge circuit. During turn-on period in every switching cycle, gate drive supply $V_g$ delivers $Q_g$ to the gate capacitance, while half of the energy $\frac{1}{2}V_gQ_g$ is stored on the gate and the other half is lost on the resistive element $R_g$. When turning off, the stored energy $\frac{1}{2}V_gQ_g$ is also lost on $R_g$. Therefore, the average gate driving power is $P_{hard} = f_sV_gQ_g$. $R_g$ is the total resistance along the charging/discharging path including resistance of $S_a$/$S_b$, internal gate resistance of the MOSFET, and any other parasitic resistance or damping resistance added by the designer. The actual $V_{gs}(t)$ would have exponential rising/falling edge, whose time constant is $R_gC_{iss}$.

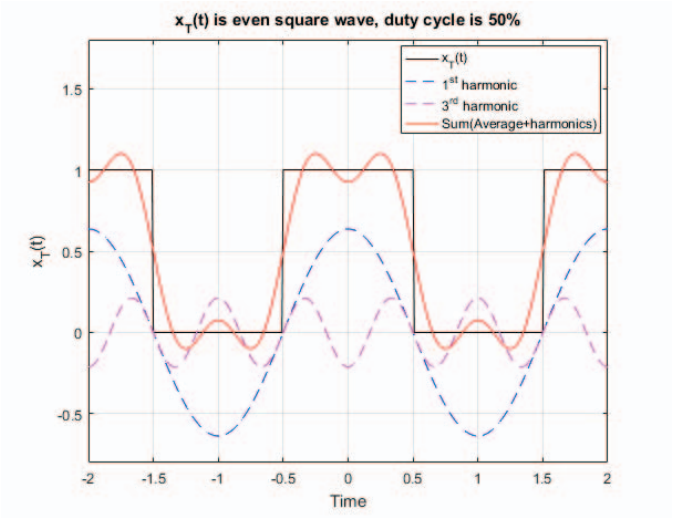



**Fig. 4:** $1^{st}$ and $3^{rd}$ Fourier series components of a $50\%$ square wave

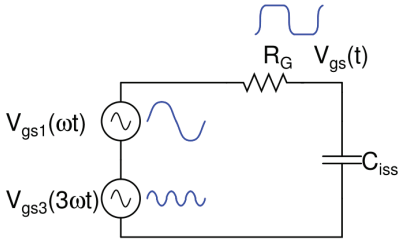



**Fig. 5:** Simplified gate drive loss model for quasi-square wave with only $1^{st}$ and $3^{rd}$ component

The conduction duty ratio of a switch in a resonant converter is typically $50\%$. The Fourier series components of a $50\%$ square wave is shown in Fig. 4. It can be seen that the summation of only the $1^{st}$ and $3^{rd}$ harmonic components can resemble closely a $50\%$ quasi-square wave. Assuming the internal gate resistance dominates $R_g$ and a quasi-square wave consisting of only $1^{st}$ and $3^{rd}$ harmonic components is used to drive the gate, the simplified circuit is shown in Fig. 5. The

gate driving loss is

$$P_{QW} = \frac{1}{2}R_g \times \left(\frac{V_g^2 A_1^2}{(\frac{1}{\omega_s C_{iss}})^2 + R_g^2} + \frac{V_g^2 A_3^2}{(\frac{1}{3\omega_s C_{iss}})^2 + R_g^2}\right) = \frac{V_g^2}{2R_g} \times \left(\frac{A_1^2}{q_s^2+1} + \frac{A_3^2}{\frac{1}{9}q_s^2+1}\right) \quad (1)$$

$q_s$ is the equivalent quality factor of the gate capacitance at the switching frequency,

$$q_s = \frac{1}{\omega_s C_{iss} R_g} \quad (2)$$

$A_1$ is the Fourier series of the 1st harmonic component, $A_3$ is the Fourier series of the 3rd harmonic component. If the duty ratio is 50%,

$$A_1 = \frac{2}{\pi}, \quad A_3 = \frac{2}{\pi} \times \frac{1}{3}, \quad (3)$$

The ratio of quasi-square wave gate driving loss over conventional hard-switching gate driving loss is

$$\frac{P_{QW}}{P_{hard}} = \frac{1}{2R_g C_{iss} f_s}\left(\frac{A_1^2}{q_s^2+1} + \frac{A_3^2}{\frac{1}{9}q_s^2+1}\right) = \pi q_s \left(\frac{A_1^2}{q_s^2+1} + \frac{A_3^2}{\frac{1}{9}q_s^2+1}\right) \quad (4)$$

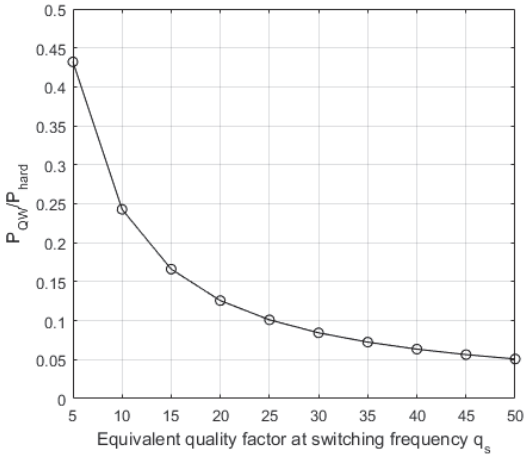



**Fig. 6:** Ratio of quasi-square gating loss and hard gating loss versus intrinsic quality factor of gate capacitance

The ratio of gate driving loss in a quasi-square gate driving circuit and a conventional hard-switching gate driving circuit, $P_{QW}/P_{hard}$, versus the intrinsic quality factor of the gate capacitance is shown in Fig. 6. For example, if the $C_{iss}$ of a MOSFET is 400 pF, $R_g = 1\ \Omega$, $V_g = 10$ V, $f_s = 20$ MHz, the intrinsic quality factor $q_s = 20$, ideally the loss would only be 12.5% of the hard-switching case. In other words, 87.5% of the gate driving loss can be saved under best case.

## III. Design Methodology

The basic idea of the proposed multi-resonant gate drive is that a conventional half-bridge circuit generates a 50% 0-$V_g$ square wave at frequency $f_s$, and then a multi-resonant circuit consisting of only passive components is connected between the switch node and the gate. This mulit-resonant circuit only passes through the $1^{st}$ harmonic component and $3^{rd}$ harmonic component to $C_{iss}$. With certain ratio of the $1^{st}$ and $3^{rd}$ harmonic components delivered to $C_{iss}$, the rising/falling time at the gate can be adjusted. Thus, the transfer function of $\frac{V_{gs}(s)}{V_{sw}(s)}$ determines the shape of $V_{gs}(t)$. In order to operate the proposed gate drive efficiently and generate a quasi-square wave $V_{gs}(t)$, two design principles of are:

1) The gate drive FETs $S_a$ and $S_b$ should operate with zero-voltage switching (ZVS) to minimize the switching losses due to the parasitic capacitance $C_{oss,a}$ and $C_{oss,b}$ in the half bridge, therefore the input impedance of this multi-resonant network $Z_{sw}(s)$ should be inductive at the switching frequency $f_s$ and other harmonic frequencies;

2) In order to shape a quasi-square wave $V_{gs}(t)$ across $C_{iss}$, the magnitudes of $1^{st}$ harmonic component $v_{gs1}(t)$ and $3^{rd}$ harmonic component $v_{gs3}(t)$ should have a ratio of $\frac{3}{1}$. The phase difference between these two harmonic components should be 0. As $V_{sw}(t)$ is already a 50% square wave, its harmonic components $v_{sw1}(t)$ and $v_{sw3}(t)$ have already satisfied this requirement. When signals of $v_{sw1}(t)$ and $v_{sw3}(t)$ pass through the circuit to $C_{iss}$, this multi-resonant "filter" should maintain the original magnitude ratio and relative phase. Therefore, the magnitude gain and phase shift of this multi-resonant "filter" at $f_s$ and $3f_s$ should be the same, in other words,

$$\frac{V_{gs}(j\omega_s)}{V_{sw}(j\omega_s)} \simeq \frac{V_{gs}(j3\omega_s)}{V_{sw}(j3\omega_s)} \quad (5)$$

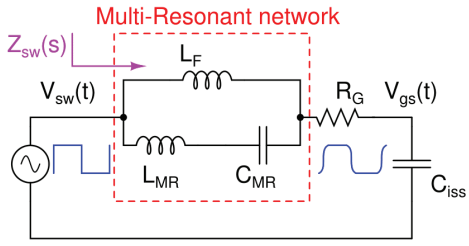



**Fig. 7:** Simplified ac circuit model

The simplified circuit for ac analysis is shown in Fig. 7. It can be treated as a square voltage $V_{sw}(t)$ driving a multi-resonant circuit, the voltage on $C_{iss}$ is $V_{gs}(t)$. The step-by-step derivation of the loading impedance $Z_{sw}(s)$ of the half bridge is shown in Fig. 8. Notice that in order for $S_a$ and $S_b$ to operate with ZVS, the impedance at $f_s$ and $3f_s$ have to be inductive. The symbolic frequency response $\frac{V_{gs}(s)}{V_{sw}(s)}$ is shown in Fig. 9. Notice that the gain at $f_s$ and $3f_s$ is 0 dB.

It can be seen from Fig. 8 that $L_F$ and $C_{iss}$ roughly resonates at $f_s$, while $L_{MR}$ and $C_{MR}$ resonates close to $3f_s$.

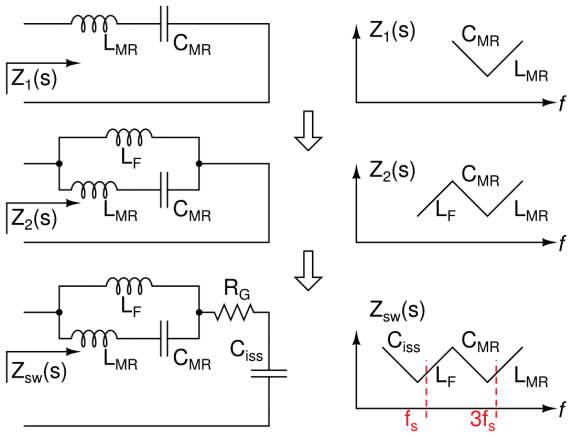



**Fig. 8:** Step-by-step derivation of $Z_{sw}(s)$, component annotated to its own impedance line, $f_s$ and $3f_s$ are placed in inductive region

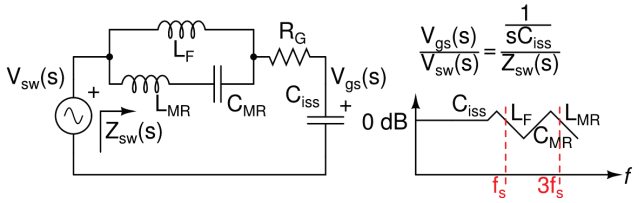



**Fig. 9:** Frequency response of the multi-resonant circuit, $f_s$ and $3f_s$ are placed at where the gain is 0 dB

Therefore, the initial values of $L_F$, $L_{MR}$, and $C_{MR}$ can be calculated by

$$L_F = \frac{1}{(2\pi f_s)^2 C_{iss}},\ L_{MR} = \frac{1}{(2\pi \cdot 3f_s)^2 C_{MR}} \tag{6}$$

$C_{MR}$ is a design parameter that can be chosen by the reader. Typically, $C_{MR} = \frac{1}{5}C_{iss}$ is a reasonable starting value. Notice, the values calculated by (6) do not meet the principles completely. Further tuning is required to achieve an ideal quasi-square $V_{gs})(t)$ and ZVS operation of $S_a$ and $S_b$.

Following the principles above, a prototype multi-resonant gate drive to generate a 0-10 V 20 MHz quasi-square wave is designed and shown here as an example. The MOSFET in the main power circuit is FDMC86248 from ON Semiconductor [15]. The $C_{iss}$ is 390 pF and $R_g$ is 0.8 Ω.
$\frac{390\ \text{pF}}{5}$ is 78 pF, so $C_{MR}$ can be chosen as 68 pF. Then

$$\begin{aligned} L_F &= \frac{1}{(2\pi \times 20\ \text{MHz})^2 \times 390\ \text{pF}} = 163\ nH \\ L_{MR} &= \frac{1}{(2\pi \times 3 \times 20\ \text{MHz})^2 \times 68\ \text{pF}} = 104\ nH \end{aligned} \tag{7}$$

Using these values calculated above, the ac simulation is shown in Fig. 10. The input impedance $Z_{sw(s)}$ is inductive at 20 MHz while capacitive at 60 MHz. After changing the inductance values, $L_F = 200$ nH, $L_{MR} = 150$ nH, the ac simulation is shown in Fig. 11. $Z_{sw(s)}$ is now inductive at both 20 MHz and 60 MHz. The gain $\frac{V_{gs}(s)}{V_{sw}(s)}$ at 20 MHz and 40 MHz are both around 0 dB, while the phase are both around $-170°$.

The transient simulation with ideal capacitor as $C_{iss}$ for both hard and resonant gating is shown in Fig. 12. The charging/discharging current supplied by $V_g$ is smaller in the proposed resonant gate driver compared to hard gating case. $R_g$ is set to be 2 Ω, which includes 0.8 Ω internal gate resistance of FDMC86248 and the output resistance from $S_a$ and $S_b$. It can be seen that the rising/falling time are similar in both cases, while the loss in proposed resonant gate drive is 180 mW and the conventional hard-switching gate driving loss is 780 mW.

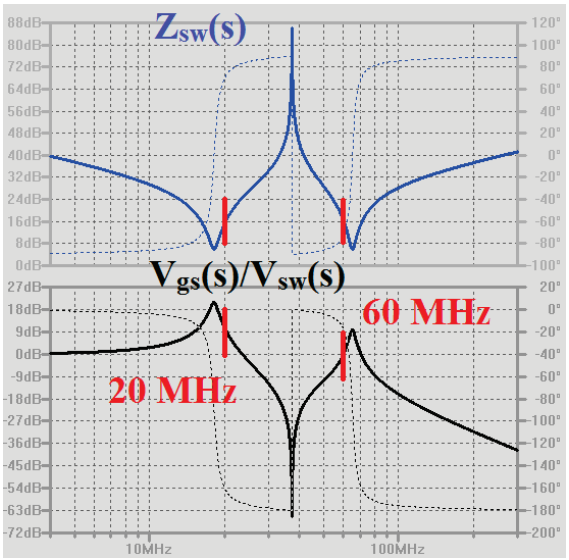



**Fig. 10:** AC simulation, ideal $C_{iss} = 390$ pF, $C_{MR} = 68$ pF, $L_F = 163$ nH, $L_{MR} = 104$ nH

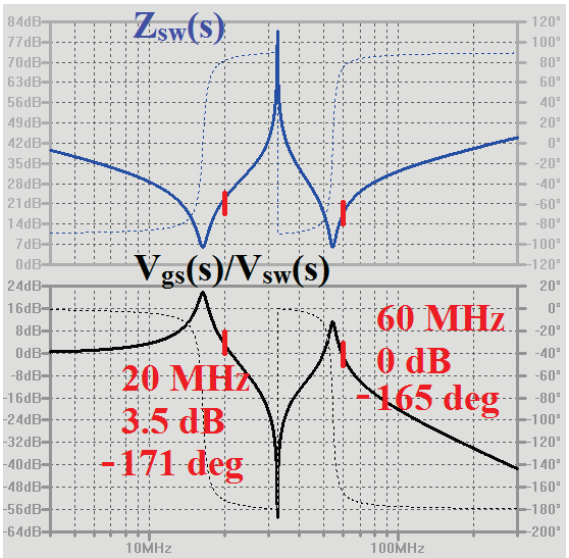



**Fig. 11:** AC simulation, ideal $C_{iss} = 390$ pF, $C_{MR} = 68$ pF, $L_F = 210$ nH, $L_{MR} = 150$ nH

## IV. Simulation and Experiments

To experimentally verify the energy saving of proposed resonant gate driver in VHF converters, two 20 MHz 32 W

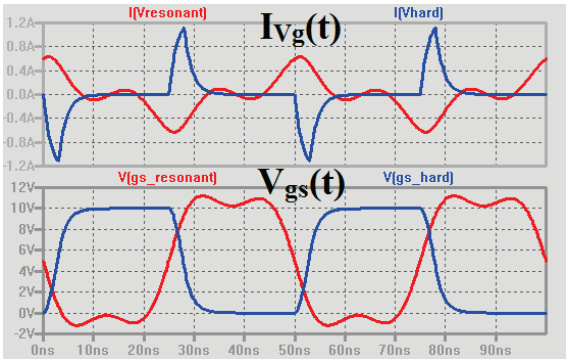



**Fig. 12:** Transient simulation with ideal $C_{iss}$, proposed multi-resonant gate drive, conventional hard-switching gate drive, top is current in gate drive supply, bottom is gate voltage

Class–E RF amplifiers with the same components are built. The circuit is shown in Fig. 13. One amplifier is driven by conventional hard-switching gate drive, while the other uses the multi-resonant gate drive designed above. The key components of the Class-E power amplifier and the resonant gate driver are list in Table I. Due to the non-linearity of the $C_{iss}$, the values of $L_{MR}$ and $L_F$ are slightly different from the values used in the transient simulation with ideal $C_{iss}$ shown in Fig. 11. Fig. 14 shows the photographs of the converters.

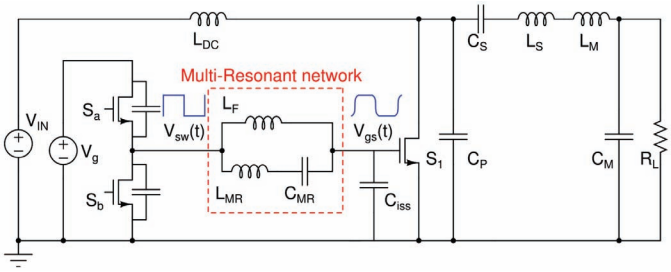
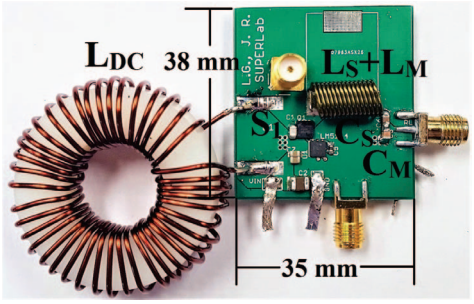



**Fig. 13:** Class–E RF amplifier with proposed resonant gate drive, $L_M$ and $C_M$ is a lowpass matching network to $R_L = 50\ \Omega$

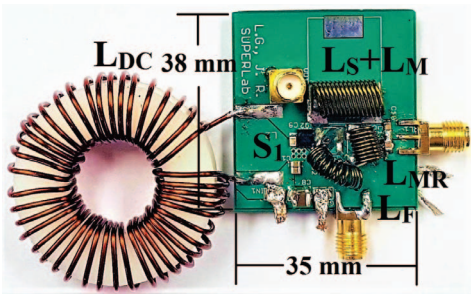
**TABLE I:** BOM of the Class–E amplifier with resonant gate driver

| Part | Value | Description |
|---|---|---|
| $V_{IN}$ | 24 V | |
| $V_g$ | 10 V | |
| $R_L$ | 50 Ω | RF attenuator |
| $L_{DC}$ | 3.3 uH | Toroid, AWG 18, 41 turns |
| $L_F$ | 181 nH | Coilcraft 132-14SMGL |
| $L_{MR}$ | 160 nH | Coilcraft 2222SQ-161 |
| $L_S$+$L_M$ | 500 nH | Coilcraft 2929SQ-501 |
| $C_{MR}$ | 68 pF | 251R15S680JV4S<br>250 V C0805 C0G |
| $C_P$ | 43 pF | 251R15S430JV4S<br>250 V C0805 C0G |
| $C_S$ | 220 pF | 251R15S221JV4S<br>250 V C0805 C0G |
| $C_M$ | 400 pF | 251R15S181JV4S<br>251R15S221JV4S<br>180 pF+220 pF<br>250 V C0805 C0G |
| $S_1$ | FDMC86248 | On Semi.,<br>150 V Si Trench MOSFET |
| $S_{a,b}$ | LM5114 | Texas Instruments gate drive IC |

The measured gate-to-source voltage waveform $V_{gs}(t)$ when the 24 Vdc input is disconnected is shown in Fig. 15. The measured $V_{gs}(t)$ in Fig. 15 is trapezoidal and closely similar to the quasi-square wave in Fig. 4 and Fig. 12.




**(a)** Class–E with hard gating




**(b)** Class–E with resonant gating

**Fig. 14:** Photographs of Class–E converters

When the Class–E amplifier is running, the measured drain-to-source voltage $V_{ds}(t)$, gate-to-source voltage $V_{gs}(t)$, and the output voltage $V_{R_L}(t)$ across the load are shown in Fig. 16. In both hard gating and resonant gating cases, $S_1$ is operating with ZVS and zero $\mathrm{d}v/\mathrm{d}t$ condition. The slower falling edge of $V_{gs}(t)$ is due to the feedback of the drain voltage through the $C_{gd}$. The measured efficiency $\eta$ of the two Class–E amplifiers are summarized in Table II.

**TABLE II:** Experimental results of prototype amplifier

| | Hard gating | Resonant gating |
|---|---|---|
| $V_{in}$ | 24 V | 24 V |
| $I_{in}$ | 1.56 A | 1.53 A |
| $V_{R_L}$ | 40.02 $V_{rms}$ | 39.78 $V_{rms}$ |
| $R_L$ | 50 Ω | 50 Ω |
| $\eta$ w/o gating loss | 85.6% | 86.1% |
| Gating loss | 1.8 W | 720 mW |
| $\eta$ with gating loss | 81.5% | 84.5% |

The proposed resonant gate drive can increase the total efficiency from 81.5% to 84.5% and saves the gating loss by 60%. Furthermore, when the gate drive IC LM5114 is loaded open circuit, it consumes 850 mW just to drive the parasitic capacitance inside the chip. This proves that the inductive impedance makes $S_a$ and $S_b$ inside the gate drive IC operate with ZVS.

Fig. 17 shows the start-up transient of the prototype converters. As predicted, the proposed resonant gate drive eliminates the long start-up time in the self-oscillating resonant gate driver in [6]. The Class–E amplifier with the proposed resonant

gate driver reaches steady state within 12 switching cycles, similar to the hard gating case.

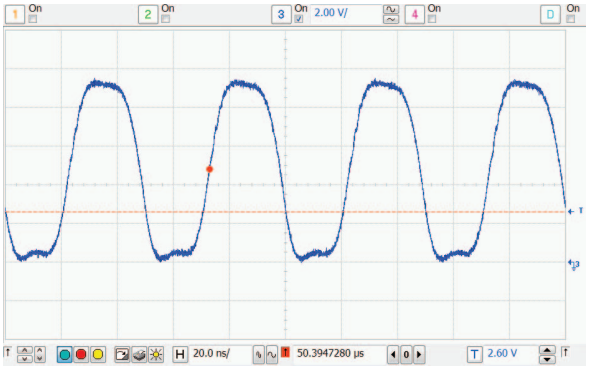
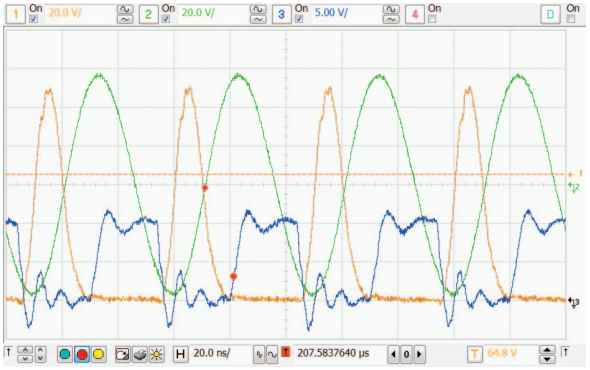
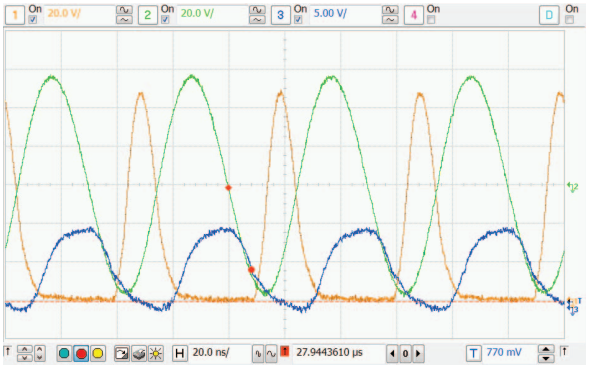


**Fig. 15:** $V_{gs}(t)$, DC input $V_{in}$ is disconnected



**(a)** Class–E with hard gating

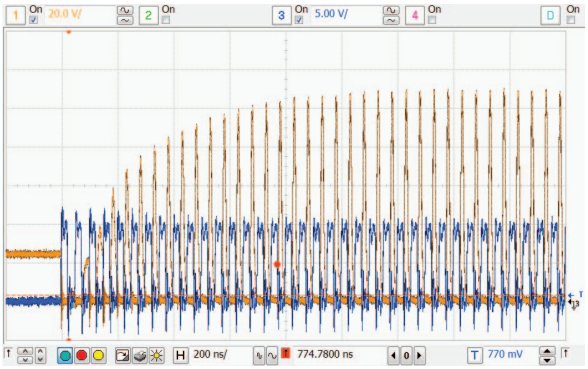


**(b)** Class–E with resonant gating

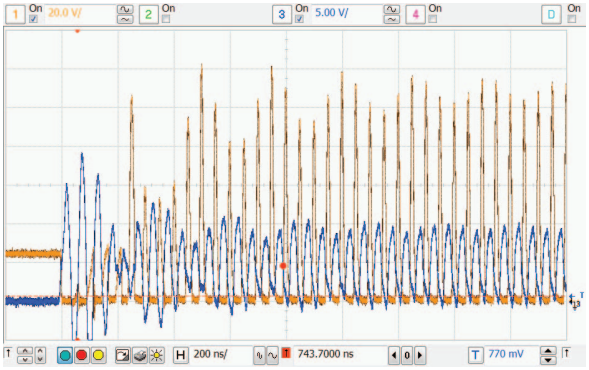
**Fig. 16:** Experimental waveform, CH1-$V_{ds}(t)$, CH2-$V_{R_L}(t)$, CH3-$V_{gs}(t)$

## V. Conclusion

A simple multi-resonant gate drive for VHF converters is presented in this paper. It drives the gate of a MOSFET with a trapezoidal quasi-square wave voltage. The design procedure is greatly simplified compared to some of self-oscillating multi-resonant gate drivers presented in previous works [6], [7], [12], [13]. The general relationship between gate energy saving percentage and intrinsic gate capacitance quality factor using a quasi-square wave resonant gate driver is analyzed. The proposed circuit eliminates the long start-up time which



**(a)** Class–E with hard gating



**(b)** Class–E with resonant gating

**Fig. 17:** Start-up transient, CH1-$V_{ds}(t)$, CH3-$V_{gs}(t)$

typically exists in a self-oscillating resonant gate driver. A prototype gate driver demonstrated the practical advantages of the proposed circuit.

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