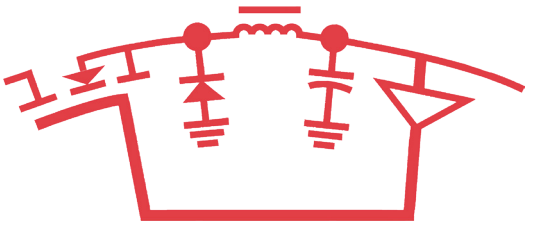

Power Supply Design Seminar

Common Mistakes in Flyback Power Supplies and How to Fix Them

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Topic 4
TI Literature Number: SLUP392

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Common Mistakes in Flyback Power Supplies and How to Fix Them

Brian King and Michael O'Loughlin

ABSTRACT

When you run into a problem in your power supply design, the odds are that someone else has already solved the same problem on another design. Wouldn't it be great if you could learn from their mistakes? This topic focuses on some of the most common mistakes in the design and troubleshooting of low-power AC/DC power supplies, specifically focusing on the flyback topology.

Presenting the material in an engaging and interactive format promotes brainstorming and the logical thought processes needed to be successful at debugging power supplies. This topic presents the symptoms of each problem, followed by possible causes, solutions and tips on how to avoid similar issues.

I. INTRODUCTION

In low power offline power supply design, typically less than 150 W, the most common power supply used is the offline flyback converter (Figure 1). These converters can be seen in AC/DC adapters for consumer electronics, cell phone and tablet battery chargers, auxiliary power supplies, etc.

There are many papers written on flyback power supply design; however, we have seen many engineers struggle with the design of these power converters. The purpose of this seminar paper is to share with the reader some real examples of what we have found to be the most common mistakes in flyback design as well as how to avoid or fix these mistakes.

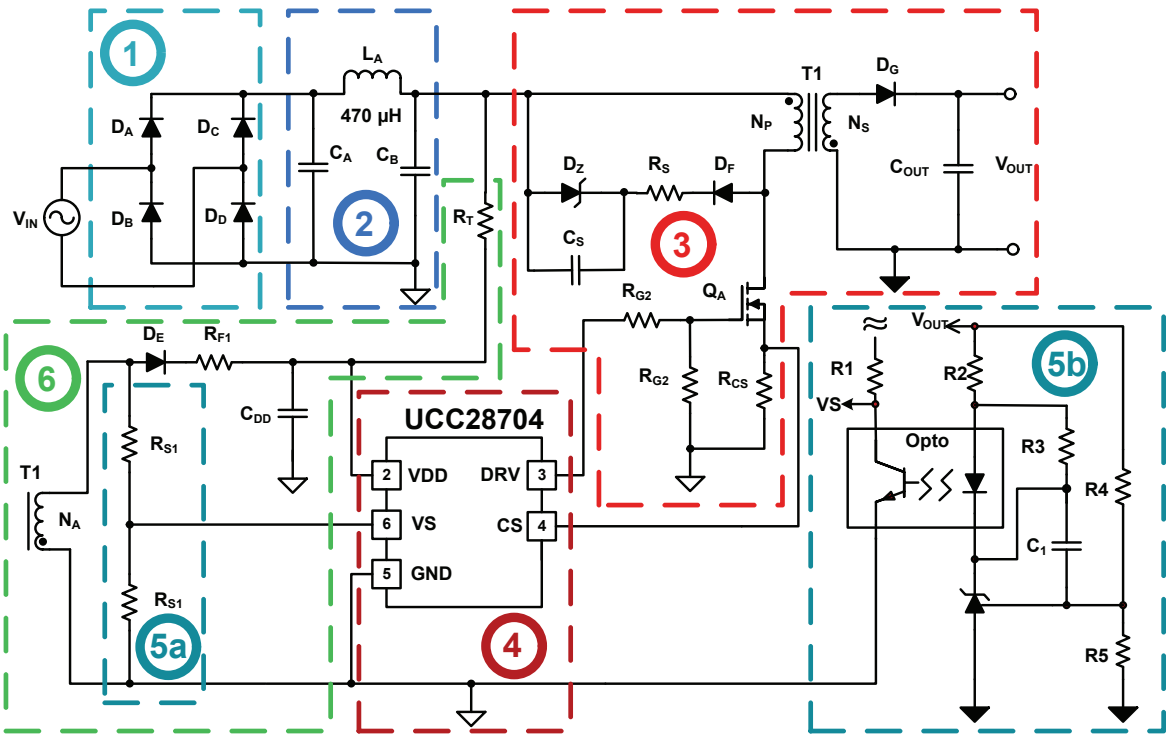

Figure 1 – Schematic of an isolated flyback converter.

Before diving into this topic, it is worthwhile to review the components and basic operation of the low power offline flyback converter. This converter uses a bridge rectifier at the input (Figure 1, Block 1) to rectify the AC line voltage and, with the aid of an input bulk capacitor (C_B), convert this AC line voltage to a DC voltage. This DC input voltage is then stepped down to a lower voltage by a flyback converter (Block 3). The flyback converter is generally controlled by a pulse width modulator (PWM) to regulate the duty cycle, switching frequency, primary current and output voltage (V_{OUT}) of the converter (Block 4). The PWM controller will require feedback circuitry to monitor the output voltage and make adjustments to the duty cycle to maintain V_{OUT}. This circuitry will consist of a TL431 error amplifier with optocoupler feedback network (Block 5b) or will use primary side regulation (PSR). PSR uses the auxiliary to secondary turns ratio (N_A/N_S) to monitor the output voltage and does not require the TL431 error amplifier/ optocoupler feedback (Block 5a). Lastly, to meet the electromagnetic interference (EMI) requirements an EMI filter (Block 2) is required.

II. Startup Issues

When powering up initial prototypes, the first problem that is encountered is often a startup issue. After an intense design effort, this can be quite frustrating, but luckily startup issues are often easily resolved. Consider the example shown in Figure 2 of a 24 V, 1 A quasi-resonant (QR) flyback converter powered from a universal AC input. In this system, there is an auxiliary circuit not shown in the schematic that requires around 3 mA from a 15 V source on the primary side of the isolation boundary. Since this power supply already generates 15 V for V_{DD} of the controller (U1), the auxiliary circuit is connected directly to V_{DD}.

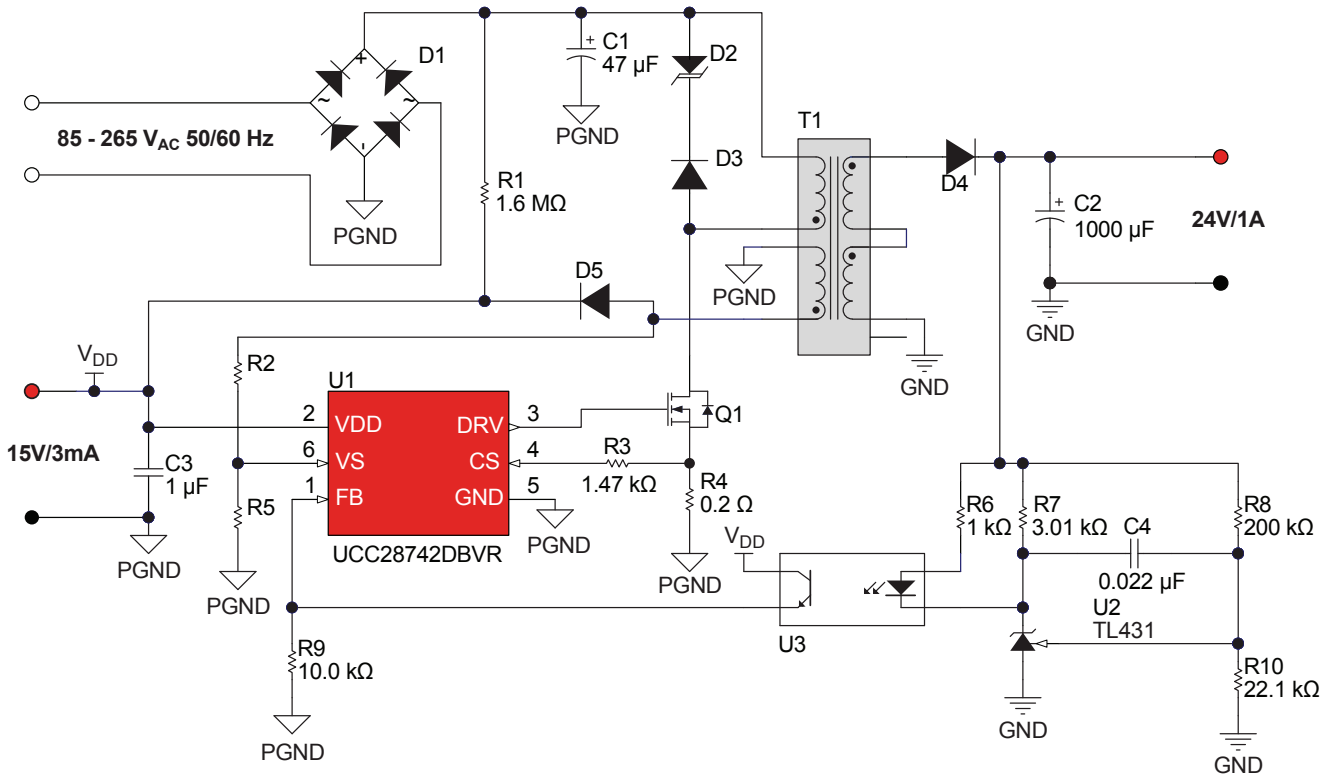

Figure 2 – Schematic of a 24 V, 1 A QR flyback converter.

At initial power up, this design did not startup. Debugging the situation, the waveforms of Figure 3 were captured. It was discovered that the output voltage is idle at 0 V and Q1 is not switching. The voltage on V_{DD} appears to be clamped at 4 V. What is preventing the controller from switching?

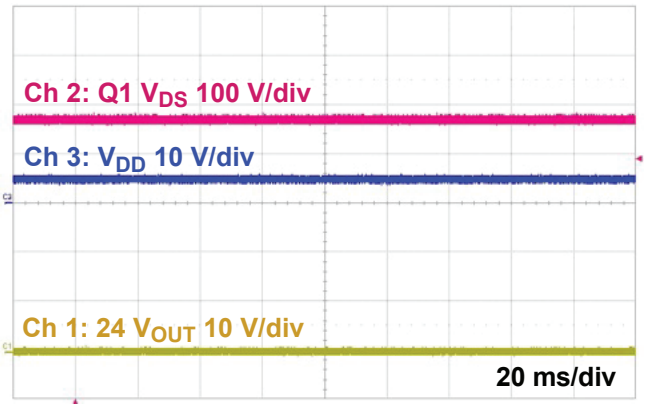

Figure 3 – Startup waveforms indicate no switching.

Before the controller can begin switching, the voltage on V_{DD} must rise above the turn-on threshold (21.6 V for the UCC28742.) The V_{DD} voltage is initially charged through resistor R1. In this case, the current through R1 is limited and the extra loading for the auxiliary circuit is preventing V_{DD} from reaching 21.6 V. One solution is to decrease the value of R1 until the controller starts. However, this will lead to excess power loss and could cause an overvoltage on the controller if the auxiliary was to turn off. A better answer is to separate the auxiliary load from the V_{DD} pin by using a separate diode from the primary bias winding of the transformer, as shown in Figure 4.

After implementing this change there are signs of life when the input power is applied, but there is still a problem. The average output voltage is only 3 V. During debug, the waveforms in Figure 5 were observed. The voltage on V_{DD} does reach the 21.6 V start threshold, and there is switching for a short period of time on the drain of Q1. But the output voltage is only rising to around 8 V before shutting down and then continually tries to restart every 70 ms. Now what is the problem?

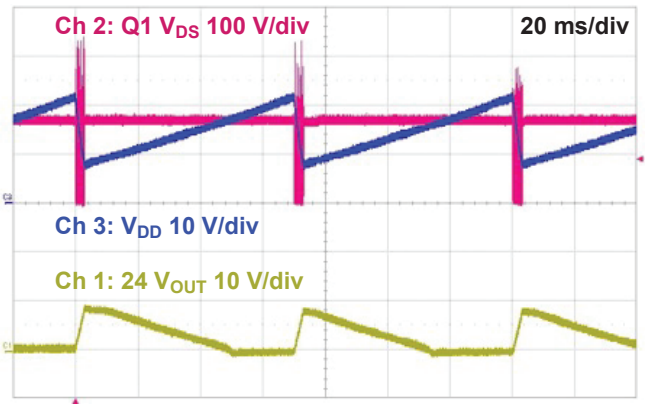

Figure 5 – Power supply is switching but still not starting up correctly.

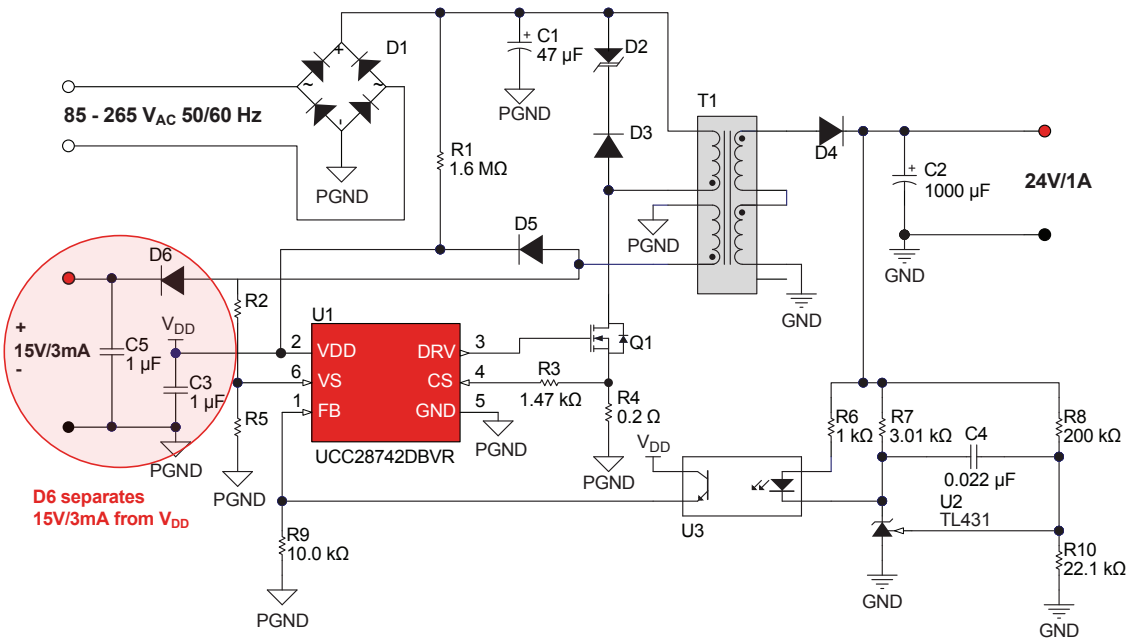

Figure 4 – Diode D6 is added to separate auxiliary load from startup circuit.

The issue is that there is not enough capacitance (C3) on the V_{DD} node. Once the controller begins switching, it draws more current from V_{DD} than is available through R1, so the voltage on V_{DD} begins to fall. C3 must supply the current during startup to hold up the V_{DD} voltage until the output voltage has risen high enough for the controller to be self-biased through the bias winding of the transformer. If the V_{DD} voltage falls to the controller's undervoltage lock out (UVLO) turn-off threshold (7.8 V for the UCC28742), the controller will stop switching. The controller will wait until V_{DD} rises above the UVLO turn-on threshold before trying to start again. The simplified diagram of Figure 6 illustrates this common startup sequence implemented by most isolated controllers [1]. The minimum required capacitance on V_{DD} is given by Equation (1).

$$C_{DD\,min} = I_{bias} \bullet \frac{t_{startup}}{UVLO_{ON} - UVLO_{OFF}} = 2.4\ mA \bullet \frac{10\ ms}{21.6 - 7.8\ V} = 1.7\ \mu F \quad (1)$$

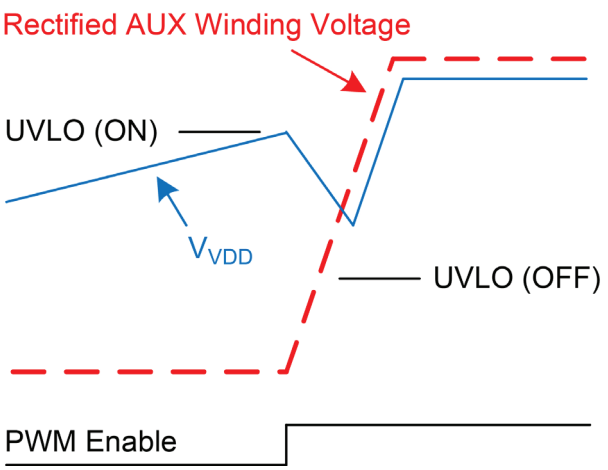

Figure 6 – Simplified startup timing diagram.

When using ceramic capacitors, be sure to consider that capacitance decreases with increasing DC bias on the capacitor. Replacing C3 with a 6.8 µF ceramic capacitor resolves the issue in this case, as shown in the waveforms of Figure 7.

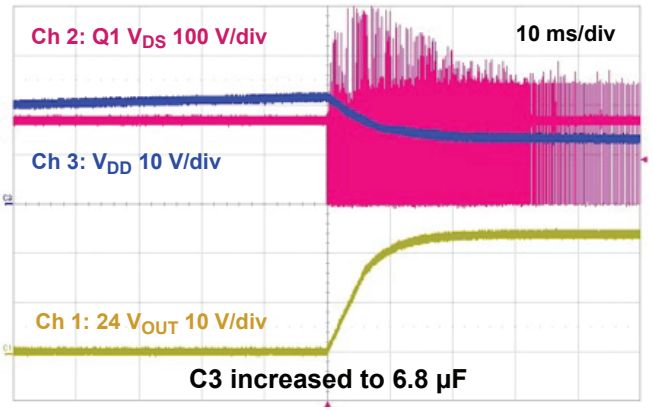

Figure 7 – Adding more capacitance to V_{DD} allows startup sequence to complete.

As illustrated here, simultaneously measuring the V_{DD}, V_{OUT} and switch node waveforms can make it easy to debug startup issues. Also be careful when the power supply needs to start with a loaded output, as the startup time can be longer if the power stage becomes current limited as the output capacitors charge.

III. Fault Protection

Most offline flyback converters provide overvoltage protection (OVP) and overcurrent protection (OCP) to prevent catastrophic failures. These two fault protections are commonly provided by simple comparators within the controller, like the example shown in Figure 8. OVP is often provided by monitoring the voltage on the auxiliary winding of the transformer, and OCP is provided by monitoring the voltage across the primary current sense resistor. Equations (2) and (3) show the calculations for the overvoltage trip point (V_{OVP}) and overcurrent trip point (I_{OCP}).

$$V_{OVP} = \frac{4.65\ V \bullet (R_{S1} + R_{S2})}{R_{S2}} \bullet \frac{N_S}{N_A} \quad (2)$$

$$I_{OCP} = \frac{1.5\ V}{R_{CS}} \quad (3)$$

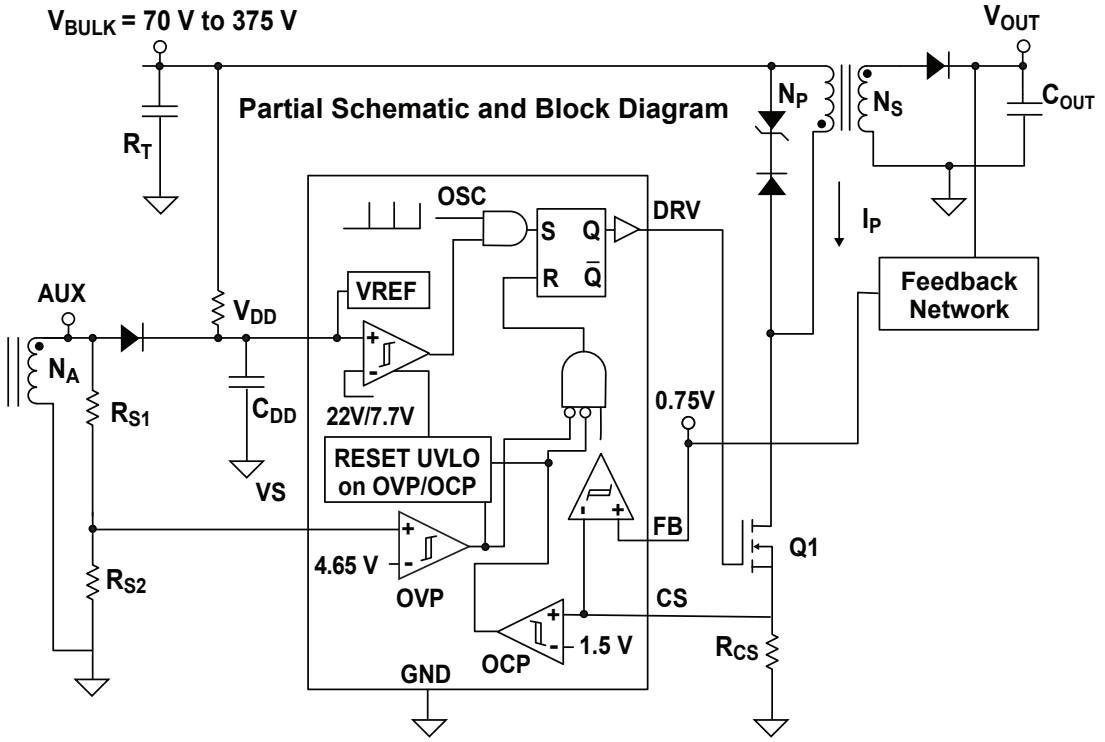

Figure 8 – OVP and OCP protection comparators.

If you are not careful, noise in the circuit can lead to unexpected circuit shutdown due to the OVP or OCP comparators being falsely triggered. Noise is most prevalent immediately after turning the primary FET on or off. To mitigate noise related issues, the inputs to the fault protection comparators are usually blanked for a short period of time after a switching event. With OCP this blanking time is typically referred to as leading edge blanking (LEB). For OVP, the blanking time is sometimes referred to as leakage reset blanking, as shown in Figure 9. Even with blanking times implemented, noise related issues can still arise as highlighted in the following two examples.

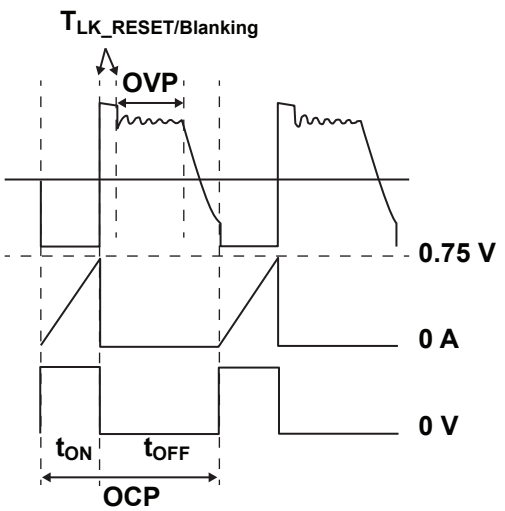

Figure 9 – Leakage blanking for OVP.

The first example uses the LM5023-2 in a 25 W QR flyback converter (Figure 10), where initial prototypes had no issues. In a later build of more units, several units began to unexpectedly shutdown after a couple of minutes operating at maximum load conditions. Three possible shutdown mechanisms for the LM5023 are OVP, OCP and UVLO on V_{CC}. The characteristics of each of these from the LM5023 data sheet are summarized in Table 1. Key waveforms to debug the problem are shown in Figure 11 and include the voltage on V_{CC} (CH1), voltage on the switch node (drain of Q2, CH2), CS pin voltage (CH3) and voltage on the QR pin (CH4). What could be causing these intermittent failures?

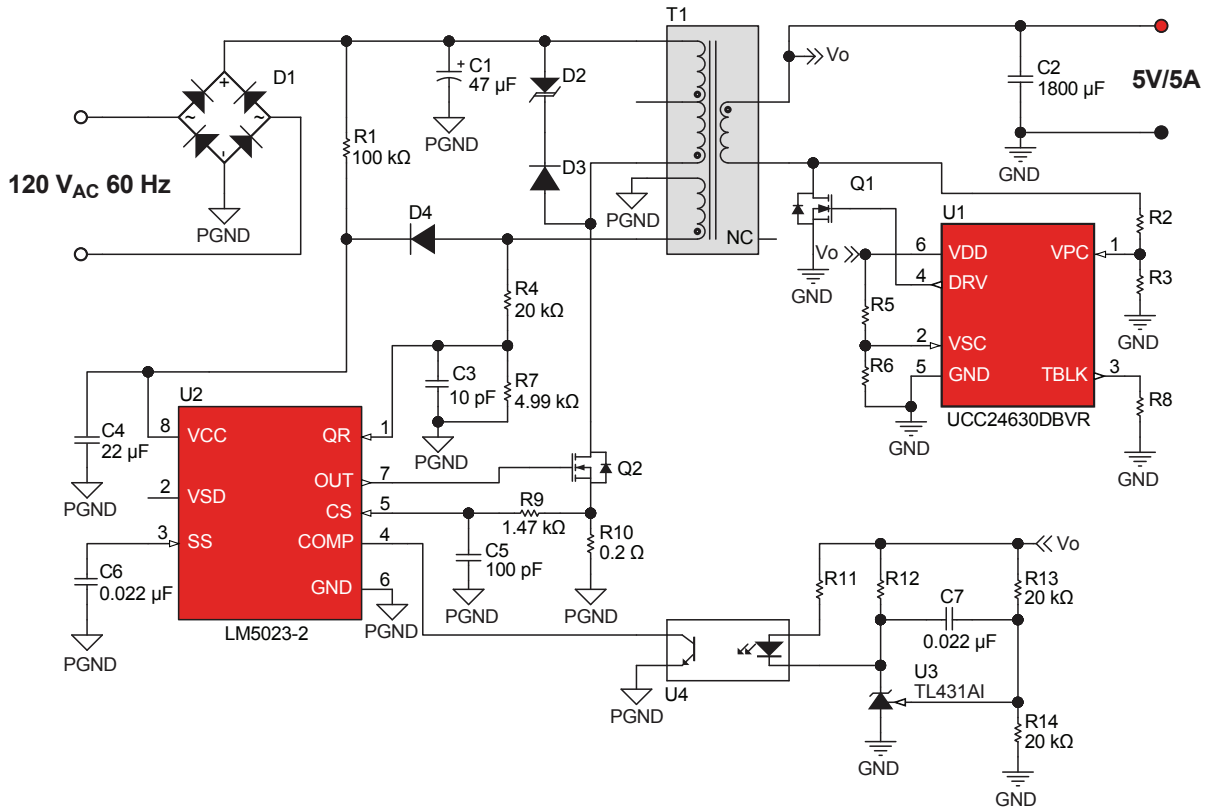

Figure 10 – LM5023 25 W QR flyback.

		MIN	TYP	MAX	Unit
Bias Supply Input					
VCC_{ON}	Controller enable threshold	12	12.8	13.5	V
VCC_{OFF}	Minimum operating voltage	7	7.5	8	V
QR Detect					
V_{OVP}	Overvoltage comparator threshold	2.85	3	3.17	V
T_{OVP}	Sample delay for OVP	870	1050	1270	ns
Current Limit					
V_{CS}	Cycle-by-cycle sense voltage limit threshold	450	500	550	mV
T_{LEB}	Leading edge blanking time		130		ns

Table 1 – LM5023 data sheet parameters.

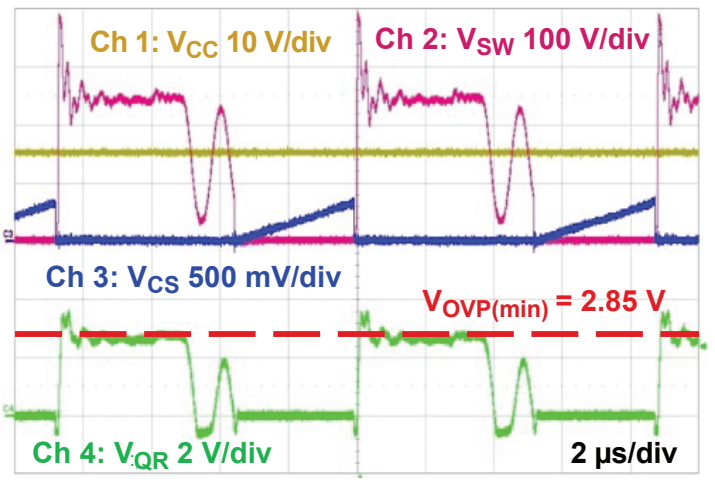

Figure 11 – LM5023 25 W oscilloscope waveforms.

From the waveforms it can be observed that V_{CC} is biased correctly and well above the 8 V turn-off threshold. The CS voltage is nowhere near the 450 mV cycle-by-cycle peak current limit (OCP). However, the QR pin voltage that is used to detect OVP is quite noisy and is near the minimum OVP threshold of 2.85 V well after the OVP sample delay time.

Clearly more margin is needed between the QR signal and the OVP trip point, and more filtering is needed to reduce the noise on this signal. However, if this signal is filtered too heavily, the waveform could be distorted and impede OVP sensing or prevent the controller from providing valley switching. In this case, decreasing the value of R7 to 4.64 kΩ reduces the amplitude of the QR signal and increasing C3 from 10 pF to 150 pF removes the noise that was causing OVP to be falsely triggered, as shown in Figure 12.

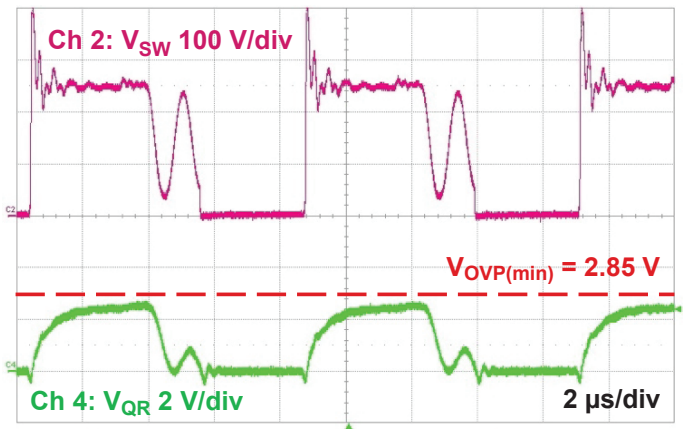

Figure 12 – OVP issue resolved by reducing the QR signal amplitude and providing more filtering.

Our second fault protection problem example is a 12 V output flyback converter using the UCC28722 with constant current (CI) constant voltage (CV) control. It is exhibiting sporadic behavior and supply shut down. Figure 13 shows how the OVP trip point on the AUX winding is not the source of the sporadic shut down. The voltage waveform across the CS resistor (V_{RCS}) is shown in Figure 14, and the OCP fault protection features of the UCC28722 are summarized by Table 2. What is causing the supply to shut down?

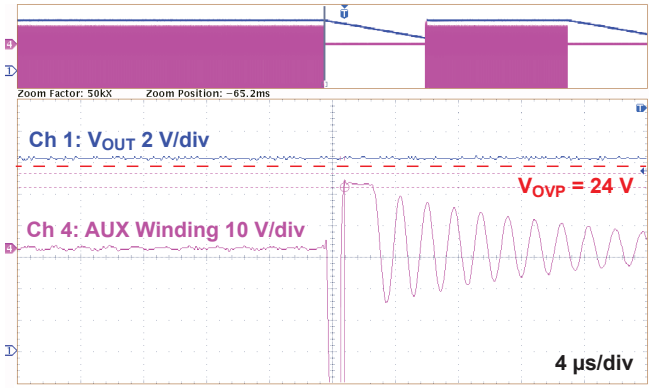

Figure 13 – Sporadic shutdown event.

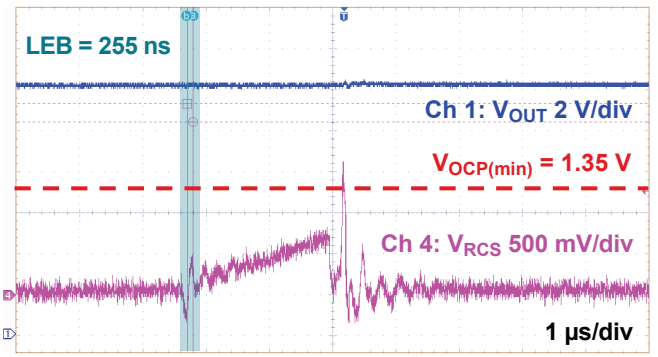

Figure 14 – Current sense voltage waveform.

The UCC28722 does provide CS leading edge blanking of 255 ns to prevent noise from falsely triggering the OCP threshold of 720 mV. However, after studying the CS waveform, we can observe a noise spike occurs across the current sense resistor (V_{RCS}, Figure 15) on the turn-off event and is tripping the OCP threshold of 1.35 V. This noise spike most likely was caused by current going through the FET parasitic capacitances due to the high dV/dt during the FET turn-off.

		MIN	TYP	MAX	Unit
CS Input					
$V_{CST(max)}$	MAX CS threshold voltage	720	750	784	mV
T_{CSLEB}	Leading edge blanking time	170	255	340	ns
Protection					
V_{OCP}	Overcurrent threshold	1.35	1.51	1.6	V
$T_{J(stop)}$	Thermal shut-down temperature		150		°C

Table 2 – UCC28722 data sheet parameters.

This problem was resolved by putting a low pass filter between the CS pin of the UCC28722 and the R_{CS} resistor. A 220 pF filter capacitor (C_f) and a resistor (R_f) of 1 kΩ were used to filter out the noise spike and stop the false OCP tripping (Figure 15).

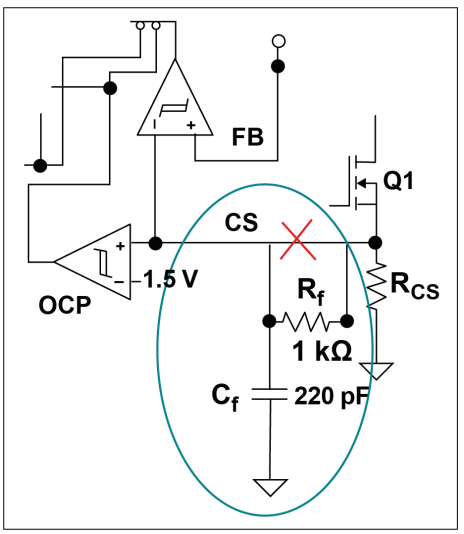

Figure 15 – Adding low pass filter to CS pin of the UCC28722.

This design had a maximum switching frequency (f_{sw}) of 72 kHz. It is recommended when setting up a filter for the CS pin that pole frequency (f_p) be at least 10 times greater than the switching frequency. The pole frequency of this design was set at roughly 720 kHz.

$$10 \bullet f_{SW} \geq f_p = \frac{1}{2\pi R_f C_f} = \frac{1}{2\pi \bullet 1\ \text{k}\Omega \bullet 220\ \text{pF}} \approx 720\ kHz$$

IV. Properly Biasing Optocoupler Feedback

The updated schematic for the 5 V, 25 W example from our OVP discussion is shown in Figure 16. With the OVP issue resolved, this power supply is now in production. After a few months, a 2% return rate is occurring from the field. The customers are complaining that the returned units would shut down after operating at heavy load for an extended period of time in a hot environment. Temperature testing on four different units, shown in Figure 17, reveals that the output voltage on the bad units increases with increasing temperature before finally shutting down. What could be the issue?

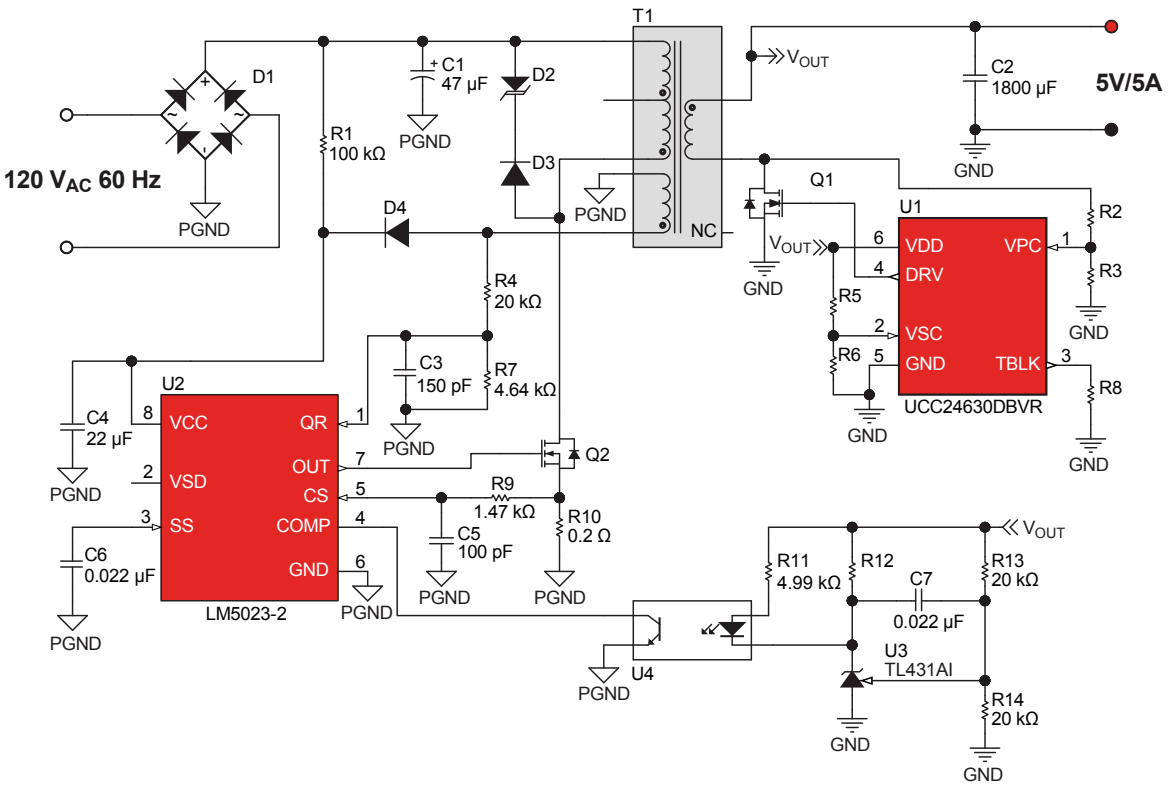

Figure 16 – Updated schematic of 5 V, 25 W QR flyback with OVP problem resolved.

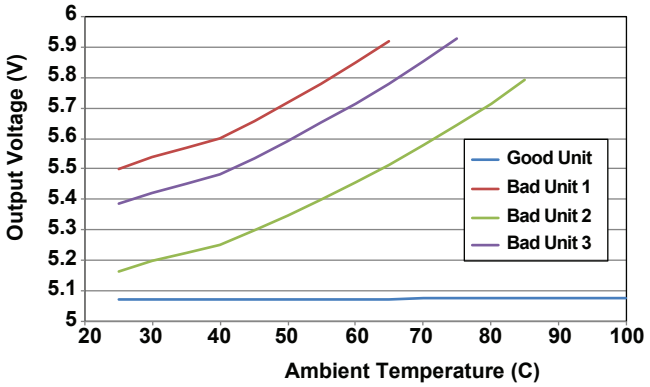

Figure 17 – Output voltage rising with increasing temperature.

The fact that a good unit remains in regulation across the entire temperature range and the bad units exhibit an increasing output voltage with temperature indicates a problem with the feedback. The most temperature sensitive component in the feedback circuitry is the optocoupler. In particular, the current transfer ratio (CTR) of the optocoupler is highly dependent on operating temperature. The CTR is the ratio of the collector current to the forward (diode) current. As the temperature increases, the CTR decreases, requiring more forward current in the optocoupler. If the R11 resistance is too high, the TL431 can't drive enough current through the optocoupler to keep the output in regulation, and the output voltage will rise.

A simplified diagram of the feedback circuit is shown in Figure 18. The first step to determining the required CTR is figuring out how much collector current is needed. This can only be found by investigating the data sheet of the controller, as all controllers are different. For the LM5023, the optocoupler must provide at least 100 µA of collector current in order to be able to pull the COMP pin to the 0% duty cycle level.

Next, calculate how much forward current is available. The minimum voltage across the TL431 (U3) is limited to around 2.5 V. With a 5 V output and assuming a 1 V forward drop across the diode of the optocoupler, that leaves only 1.5 V across R11. If R11 is set to 5 kΩ, only 300 µA is available to drive the optocoupler.

Finally, the minimum CTR needed for a given value of R11 can be calculated by dividing the maximum collector current needed by the minimum forward current available.

$$CTR \geq \frac{I_{Cmax}}{I_{Fmin}} = \frac{100\ \mu A}{300\ \mu A} = 0.33 \text{ for } R11 = 5\ k\Omega$$

The problem becomes apparent when we investigate the normalized CTR curves of the optocoupler used in this design, as shown in Figure 19. The red dot denotes the 300 µA of forward current operating condition, which is barely along the curve lines of available CTR at 25°C and below. The problem is even worse, considering that the CTR of an optocoupler is also dependent on initial tolerance and degrades with life [2]. The solution, however, is simple. The value of R11 can be reduced until enough forward current is provided to sufficiently bias the optocoupler. In this example, reducing R11 to 2 kΩ provides at least 750 µA and requires a minimum CTR of only 0.13. This is denoted by the blue dot in Figure 19, which is well within the capabilities of the chosen optocoupler.

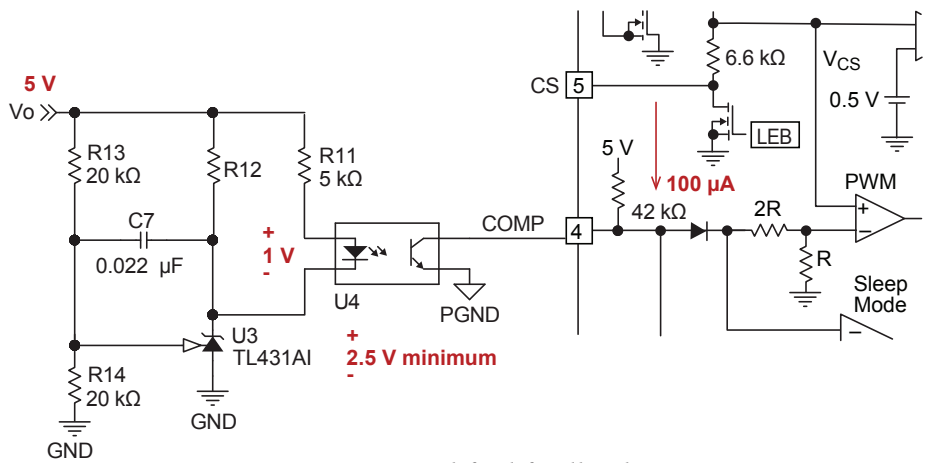

Figure 18 – Simplified feedback circuit.

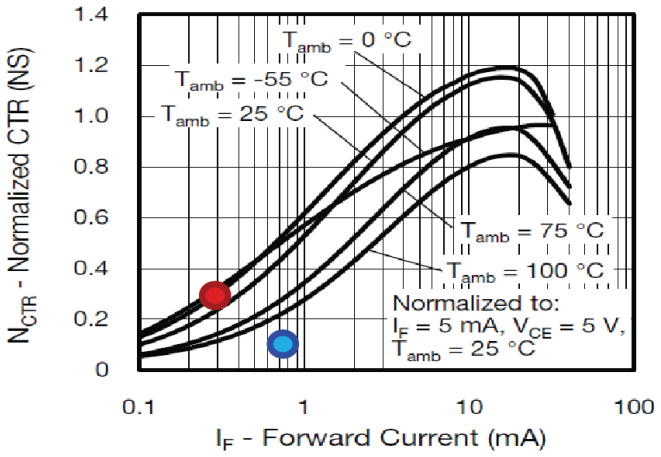

Figure 19 – Normalized CTR and minimum CTR needed for R11 of 5 kΩ (RED) and 2 kΩ (BLUE).

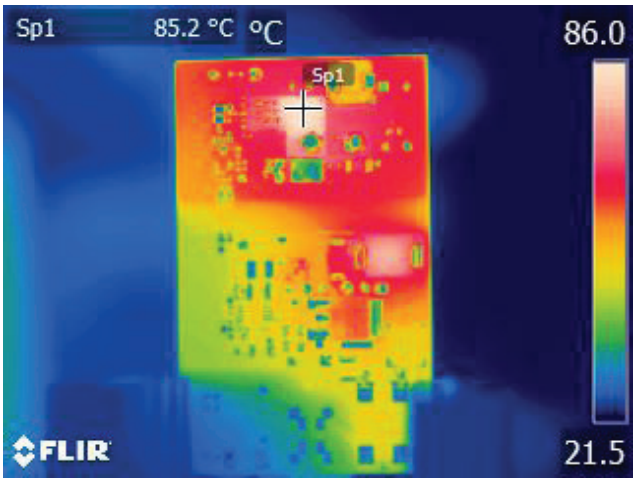

Figure 20 – Thermal image reveals SR is getting hotter than expected.

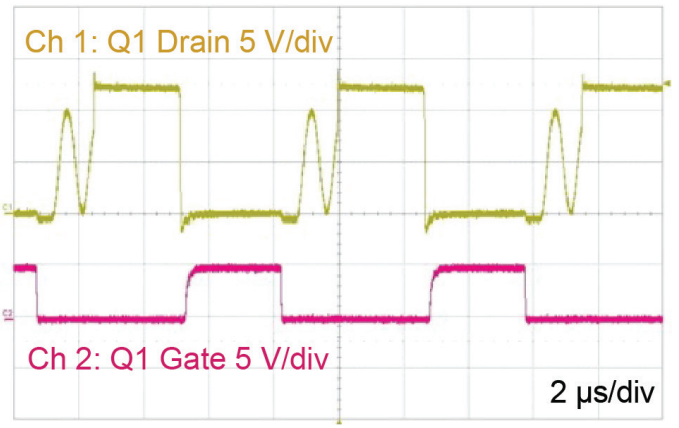

Figure 21 – SR voltage waveforms.

V. Selecting and Driving MOSFETs

Replacing the output diode in a flyback converter with a MOSFET, also referred to as a synchronous rectifier (SR), can greatly improve efficiency, particularly in applications with higher output current. Our 5 V output 25 W LM5023 example uses an SR (Q1 in Figure 16) to improve efficiency. The average value of the SR current is equal to the DC output current, or 5 A. However, because the supply operates in discontinuous conduction mode (DCM), the RMS value of the secondary current is much higher due to its triangle-wave shape and is approximately 10 A_{RMS}. If a Schottky diode is used with an assumed forward voltage drop of 0.5 V, we expect approximately 2.5 W of loss in the rectifier. This is difficult to manage thermally and severely impacts the efficiency. Instead, a FET with an on-resistance of 3.5 mΩ is used, and we expect around 350 mW of conduction loss. However, when we look at the thermal plots in Figure 20, the SR is getting much hotter than expected at around 85°C. Why is the SR getting so hot?

The first thing you might suspect is that the UCC24630 SR driver is not providing any gate pulses to the SR. If there were no drive to the SR, all of the secondary current would flow through the body diode of the SR rather than through the FET channel, which would explain this higher than expected temperature. However, as the waveforms of Figure 21 indicate, the SR is being driven and is turning on. Some information from the SR FET data sheet is provided in Table 3 and Figure 22.

T_A=25°C		Typical Value		Unit
V_{DS}	Drain-to-source voltage	60		V
Q_g	Gate charge total (10 V)	49		nC
Q_{gd}	Gate charge gate-to-drain	7.9		nC
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 6 V	3.5	mΩ
		V_{GS} = 10 V	2.7	
$V_{GS(th)}$	Threshold voltage	2.8		V

Table 3 – SR data sheet information.

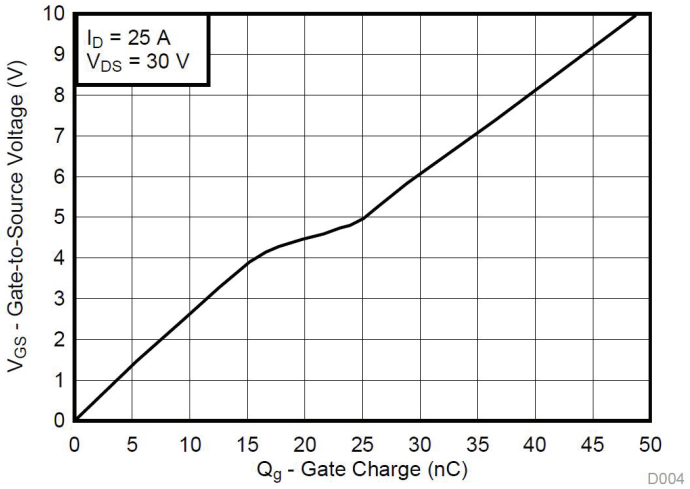

Figure 22 – Gate-to-source voltage versus gate charge.

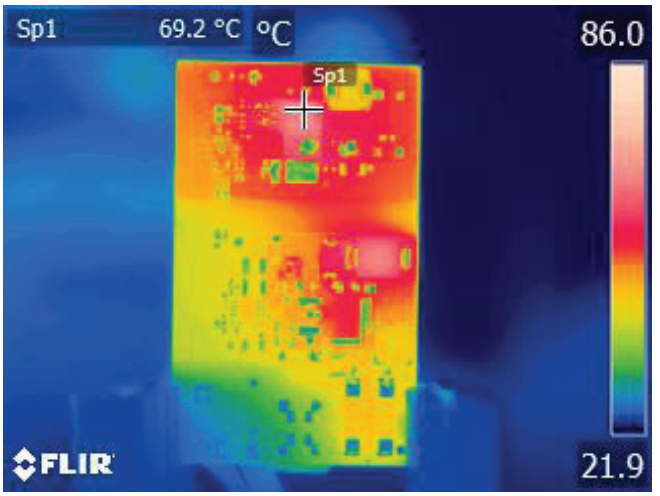

Figure 23 – SR with 5 V optimized drive reduces case temperature by 16°C.

The UCC24630 derives its V_{DD} from the 5 V output, so the drive voltage is limited to 5 V. Even though this is enough to turn the SR on, the SR is not fully enhanced. The Miller plateau can be seen in Figure 22 and is just below 5 V. Another clue is that the 3.5 mΩ on-resistance in Table 3 is specified at 6 V. No data is provided for this FET with a 5 V drive. When selecting a FET for any application, it is important to ensure that it is fully enhanced at all operating conditions. By replacing the SR FET with one designed to operate with a 5 V drive, like the one summarized by the data in Table 4, the thermal performance and efficiency can be improved, as shown in Figure 23.

T_A=25°C		Typical Value		Unit
V_{DS}	Drain-to-source voltage	30		V
Q_g	Gate charge total (4.5 V)	39		nC
Q_{gd}	Gate charge gate-to-drain	9.3		nC
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V	1.15	mΩ
		V_{GS} = 10 V	0.95	
$V_{GS(th)}$	Threshold voltage	2.8		V

Table 4 – SR better suited for 5 V drive.

You may have also suspected that there was cross-conduction between the primary FET (Q2) and the SR (Q1). However, this can't happen in a flyback operating in QR mode or DCM. This is because the QR controller will not apply a gate pulse to the primary controller until it has detected that the output rectifier has turned off. If this flyback converter was operating in continuous conduction mode (CCM), cross-conduction would be a legitimate concern. In CCM, it is often desirable to slow down the turn-on of the primary FET by adding a simple gate resistor to the drive path like that shown in Figure 24(a). Slowing down the turn-on of the primary FET gives the output rectifier more time to turn off and limits the amplitude of any resulting current spikes. However, the gate resistor will also slow down the turn-off of the primary FET and can increase turn-off switching loss. In CCM flybacks, adding a simple reverse parallel diode (Figure 24(b)) or PNP transistor to ground (Figure 24(c)) can maintain the slow turn-on path and speed up the turn-off path.

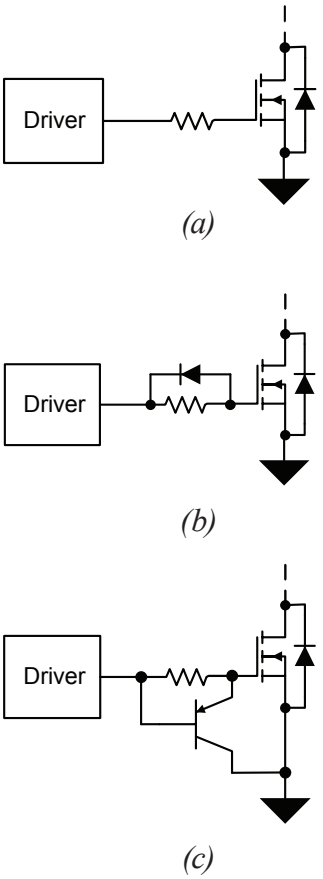

Figure 24 – Simple techniques to control FET slew rates.

VI. Managing Loss in the Primary Clamp

In a flyback converter, when the primary FET is on, the primary magnetizing and leakage inductances are charged up to the peak primary current level. When the primary FET turns off, the magnetizing energy is coupled and delivered to the output through the secondary winding of the transformer. The leakage inductance is not coupled to the secondary, so a mechanism needs to be provided to discharge the leakage energy without damaging the primary FET. This is commonly accomplished with a passive clamp, like D4 and D2 in the 24 V, 36 W DCM flyback shown in Figure 25. When the primary FET turns off, the inductive leakage energy temporarily forward biases D4. D2 limits the voltage on the drain of Q1 to a level equal to the input voltage plus the clamping voltage of D2. D4 continues to conduct until the current in the leakage inductance reduces to zero.

This design has a primary to secondary turn ratio of 4:1, 4 µH of leakage inductance and 200 µH of magnetizing inductance. The primary voltage and current waveforms are shown in Figure 26. The efficiency of this design is not bad at 88.8%, but D2 is getting too hot as shown in Figure 27. What can be done to lower the temperature of D2?

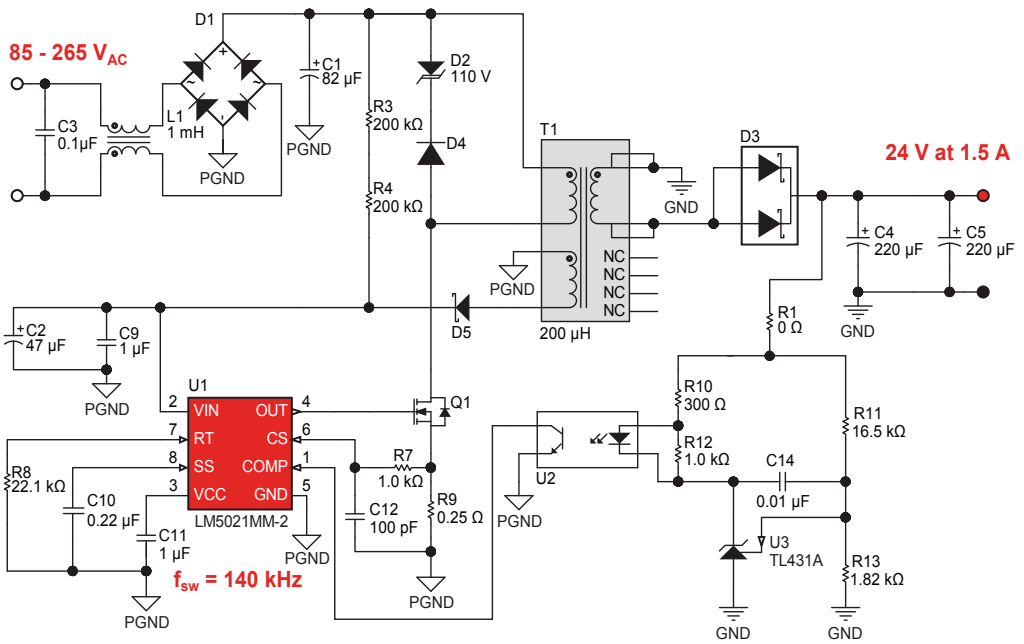

Figure 25 – A 24 V, 36 W DCM flyback.

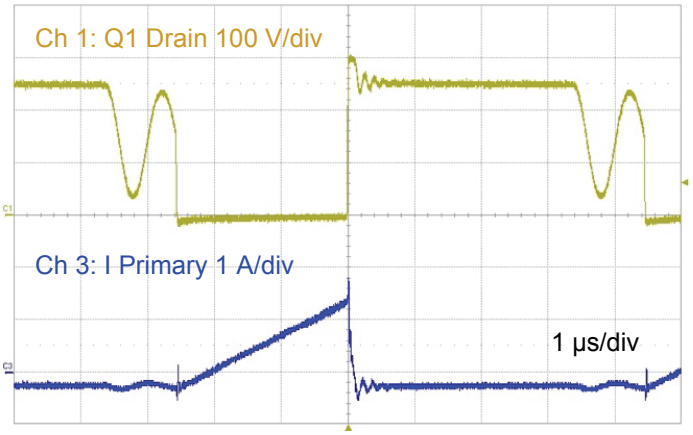

Figure 26 – Primary voltage and current waveforms with 115 V_{AC}, 60 Hz input and 1.5 A load.

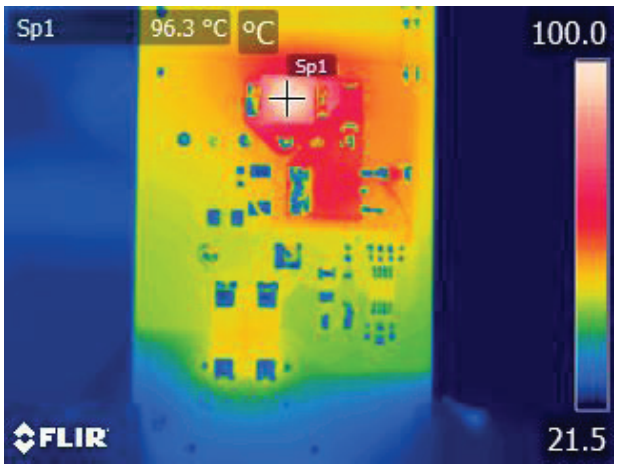

Figure 27 – Clamping TVS is too hot.

Reducing the leakage inductance is perhaps the most obvious answer, because most of the leakage energy is dissipated in the clamp. What is not so obvious is that in addition to the leakage energy, a portion of the magnetizing energy is dissipated in the clamp while D4 is conducting [3, 4]. Therefore, it is important to discharge the leakage inductance as quickly as possible. Reducing the leakage inductance will help speed up the discharge time too. The design has a 2% ratio of leakage inductance to magnetizing inductance, which is not bad. It is possible that by redesigning the transformer this could be reduced a little further. In general, a 1% ratio is very good, but could be difficult to achieve. What else could be done to speed up the leakage reset time?

While D4 is conducting, the voltage across the leakage inductance is equal to the clamping voltage of D2 minus the output voltage reflected to the primary winding. By increasing the clamping voltage, we can apply a higher voltage across the leakage inductance to discharge it faster, but be careful not to exceed the maximum drain-source voltage rating of the FET. By simply replacing D2 with a 150 V TVS, the leakage reset time is dramatically reduced as shown in the new waveforms of Figure 28. The efficiency is now improved to 89.7% and the temperature of the clamp is reduced by over 15°C as shown in Figure 29.

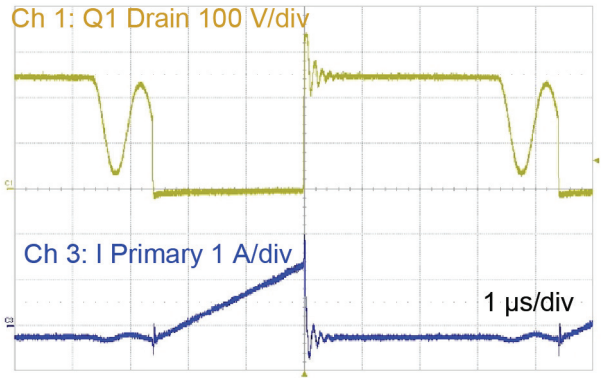

Figure 28 – Higher clamping voltage speeds up the leakage reset time.

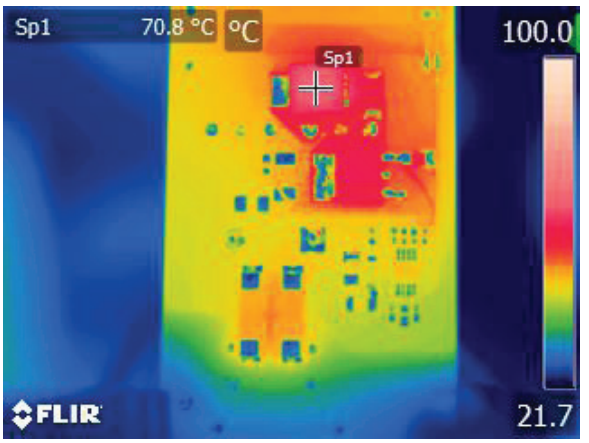

Figure 29 – Faster leakage reset reduces loss in clamp.

A capacitor with parallel power resistors can be used for clamping instead of a TVS. Assuming the capacitor-resistor clamps at the same voltage as the TVS, there would be no difference in the power loss of the clamp or overall efficiency. Using power resistors may be less expensive and provides a way to spread the heat to reduce the

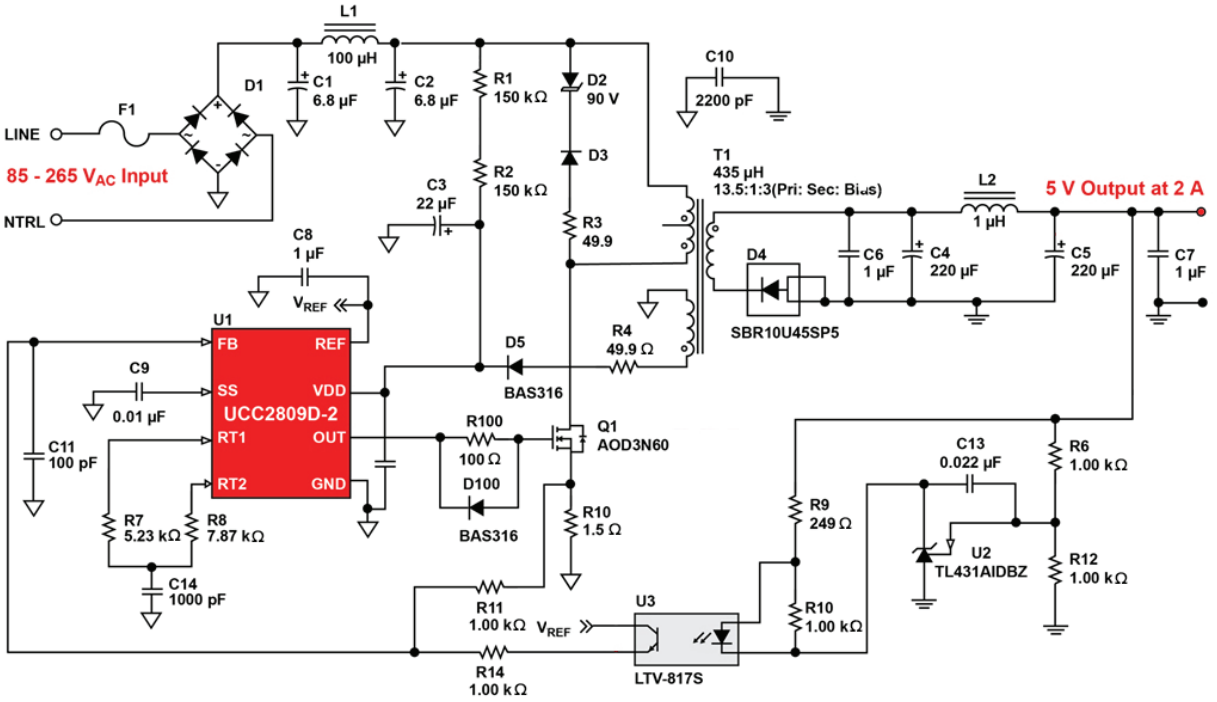

Figure 30 – 5 V, 10 W flyback converter.

maximum temperature. The advantages of a TVS are that it is a single component and clamps at a controlled voltage. The clamp voltage of the capacitor-resistor will change with line and load.

There are many other forms of the flyback converter that recycle the leakage energy for higher efficiency, like the two-switch flyback and active-clamp flyback. The trade-off for these more efficient flyback converter variations is higher cost and complexity. There are also some lossless clamps that can be implemented which come with trade-offs of limited duty cycle or higher voltage stress on the switches, in addition to higher cost [5, 6].

VII. Minimizing Standby Power

Having high efficiency at maximum load is no longer good enough in many applications. New industry consortiums and governmental regulations are promoting low power loss at fractional loads and at standby (no load). For example, the European Union Code of Conduct (CoC) Tier 2 specification for external power supplies under 50 W says a power supply must not consume more than 75 mW with no load attached. You must pay close attention to every mW of loss in order to meet these strict requirements. Take for example the 5 V, 10 W flyback converter shown in Figure 30. The no load power loss versus input voltage is shown in Figure 31. The power loss at 85 V_{AC} input is twice the 75 mW specification and quickly grows to 600 mW at 230 V_{AC}, where the CoC input power measurement needs to be taken. What changes can be made to improve the no load performance?

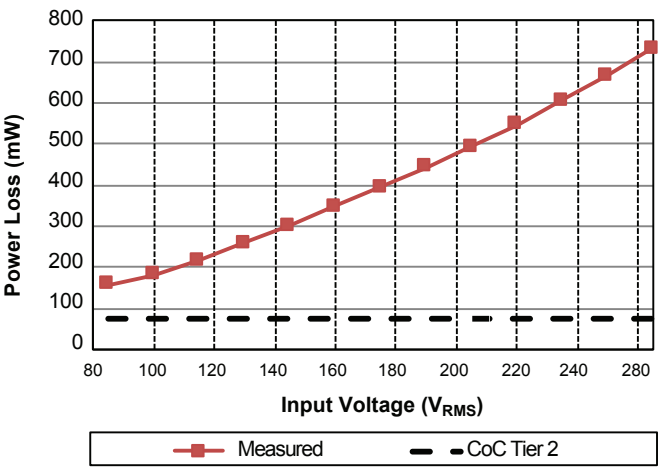

Figure 31 – Poor standby power loss performance.

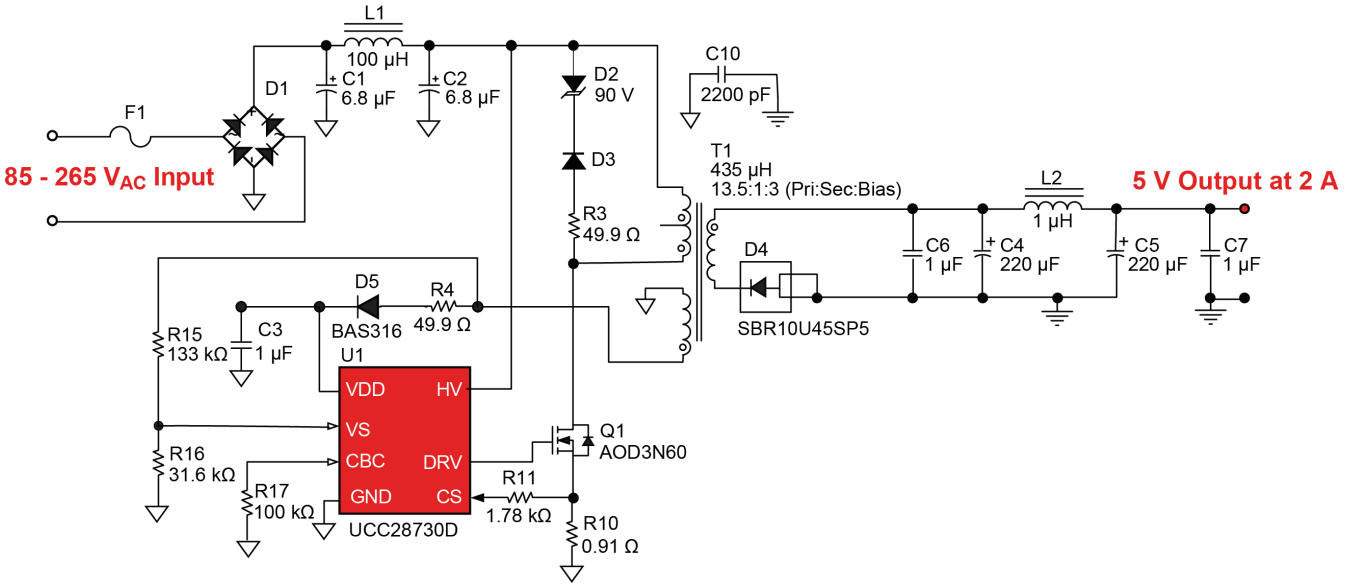

Figure 32 – 5 V, 10 W flyback redesigned for lower standby power consumption.

A major portion of the standby losses is due to the loss in the startup resistors, R1 and R2. These resistors contribute over 300 mW to the standby loss at 230 V_{AC} input. The total resistance in this path needs to be low enough to provide the startup current of the controller, so that the power supply is guaranteed to start at minimum input, but should otherwise be kept as high as possible to limit power dissipation. Selecting a control IC with low start-up current will help reduce this loss. Even better, some controllers have active startup circuits which turn off the startup current and completely eliminate this loss source.

The controller shown in Figure 30 operates at a fixed 100 kHz switching frequency. Every time the main FET (Q1) turns on, the parasitic switch-node capacitance from the drain to ground is discharged, and the energy that was stored in this capacitance is burned as loss in the FET. As the load is decreased, these switching related losses become a larger percentage of the overall loss. Modern controllers mitigate this problem by implementing different operating modes to reduce the switching frequency or operate in a burst mode at light loads. Selecting a controller optimized for light load efficiency is crucial for complying with modern efficiency initiatives [1].

Reducing the total switch-node capacitance will further reduce standby power consumption. The output capacitance of Q1 is typically the largest contributor to the switch-node capacitance. The switch-node capacitance also includes the junction capacitance of the output diode (D4) reflected from the secondary windings to the primary winding and the transformer winding capacitance. Selecting a FET with low output capacitance and a diode with low junction capacitance will help reduce standby power consumption.

The circuit of Figure 32 shows the same power supply redesigned using the UCC28730 for lower standby power consumption. This device has an integrated startup circuit, which eliminates losses in the startup resistors R1 and R2. The UCC28730 also allows the switching frequency to drop as low as 30 Hz at no load to minimize switching related loss. In addition, this controller uses primary side regulation (PSR), which eliminates the optocoupler and TL431 (U2) regulating circuit. The power loss in the TL431 regulating circuit is on the order of 10 to 20 mW but could make the difference between passing standby power design requirements or not passing them. These changes reduce the standby power consumption below 20 mW total, as shown in Figure 33.

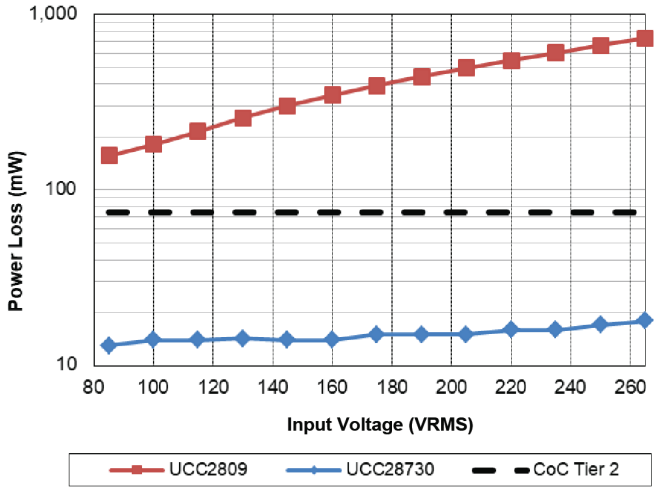

Figure 33 – Improved standby performance.

VIII. PCB Layout

A poor layout can ruin a perfectly good power supply design. Take for example the 200 mW PSR flyback converter shown in Figure 34. This supply works fine at no load, but when load is applied the output goes out of regulation and the supply switches erratically. After inspecting the current sense signal (Figure 35), undesirable voltage spikes are seen on the waveform. The large positive spike is blocked by the leading edge blanking, but the large negative spike exceeds the maximum negative voltage rating for the CS pin. This can inject currents into the substrate and cause erratic behavior or even device failure.

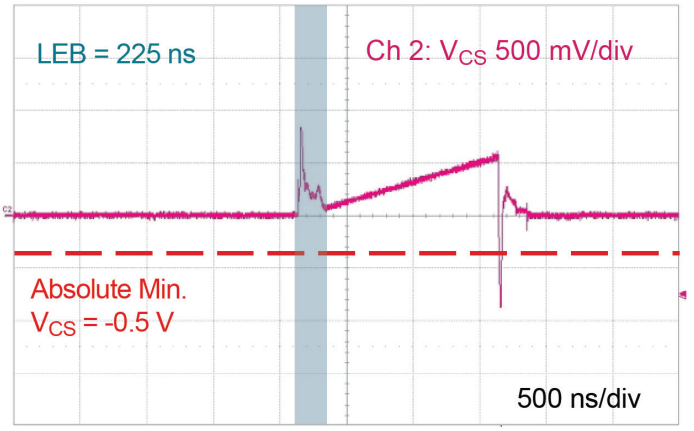

Figure 35 – Large spikes on the current sense voltage.

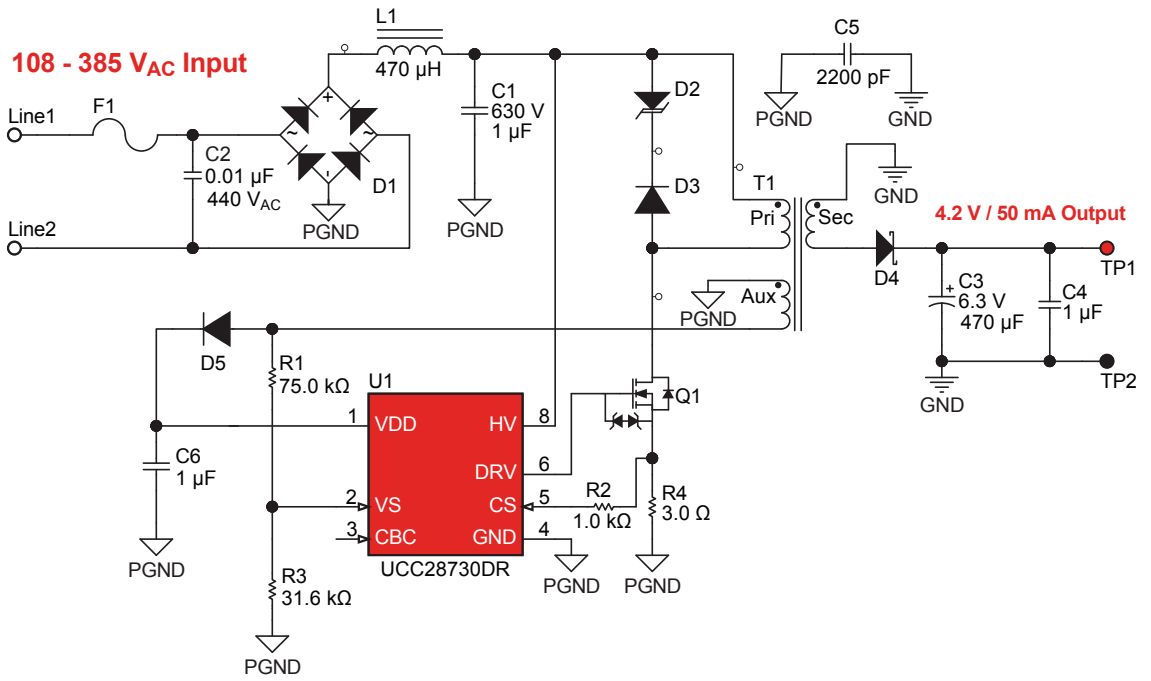

Figure 34 – A 4.2 V, 200 mW isolated flyback converter.

The PCB is routed on two layers, as shown in Figure 36, with the current sense and primary current return path shown by the thick curved arrows. The majority of the routing is on the bottom layer, and primary ground (PGND) is also poured on the bottom layer. The islands of unconnected PGND on the bottom layer are tied together by a trace on the top layer. How can this layout be improved to eliminate the noise on the current sense?

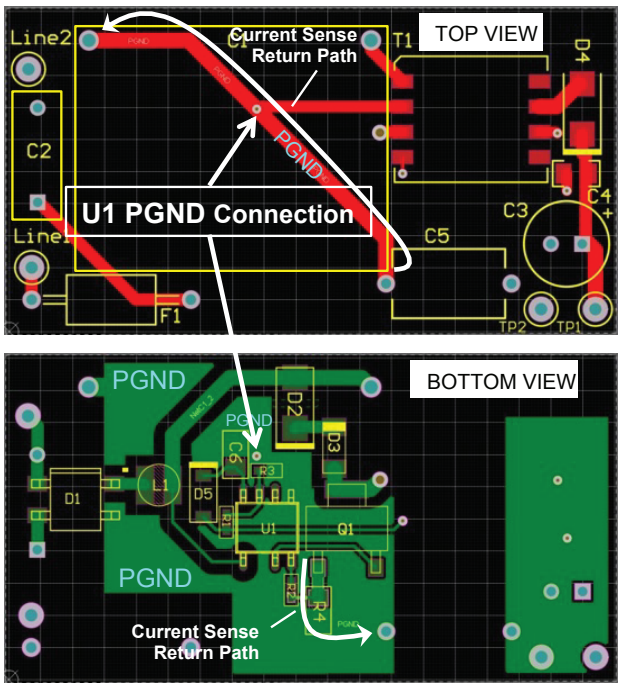

Figure 36 – Poor layout causing noise on CS signal.

With the very segmented PGND on the bottom layer, the switching current can only return to the bulk capacitor through a long power ground (PGND) trace on the top layer. This long trace introduces an inductance to the return path for the switching current. The controller (U1) PGND connection is in the middle of the top layer trace. When the switch turns off, this inductance induces the large negative voltage spike.

Figure 37 shows an improved layout. The components on the bottom side were moved so that the current sense resistor (R4) is closer to the PGND connection of the input capacitor (C1). This reduces the inductance in the return path. The controller (U1) is placed away from the noisy return path of the switching currents. PGND is flooded in the dead space on both the bottom and top layers and stitched together with vias near intruding traces. This minimizes ground noise, provides some shielding and helps to spread heat.

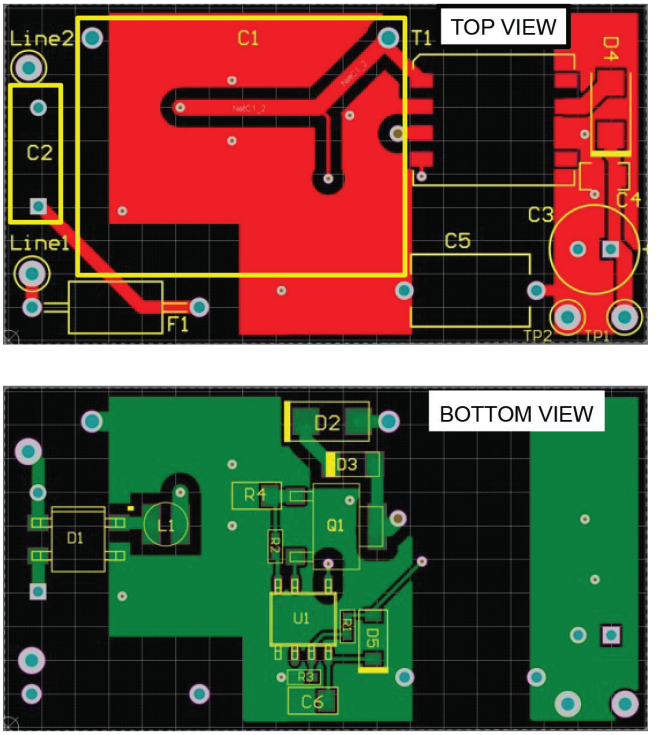

Figure 37 – Modified layout to reduce noise on CS.

PCB layout is a complex topic with many subtleties but following a few simple rules can help reduce parasitic elements and improve the performance of your power supply [7].

First, reduce parasitic inductances by keeping the current loops as small as possible. Use ground planes under your signal and power traces whenever possible. Place IC filter capacitors as close to the IC pins as possible.

Second, reduce parasitic capacitance by minimizing the cross sectional area of the switch node and grounding heat sinks. Cross traces on adjacent layers orthogonally, which not only reduces parasitic capacitance but also prevents inductive current coupling in your traces.

Third, reduce parasitic resistance by placing your power components as close as possible. Make sure your high current circuit paths are as short as possible. Use wide etches on high current paths to reduce trace impedance and improve efficiency.

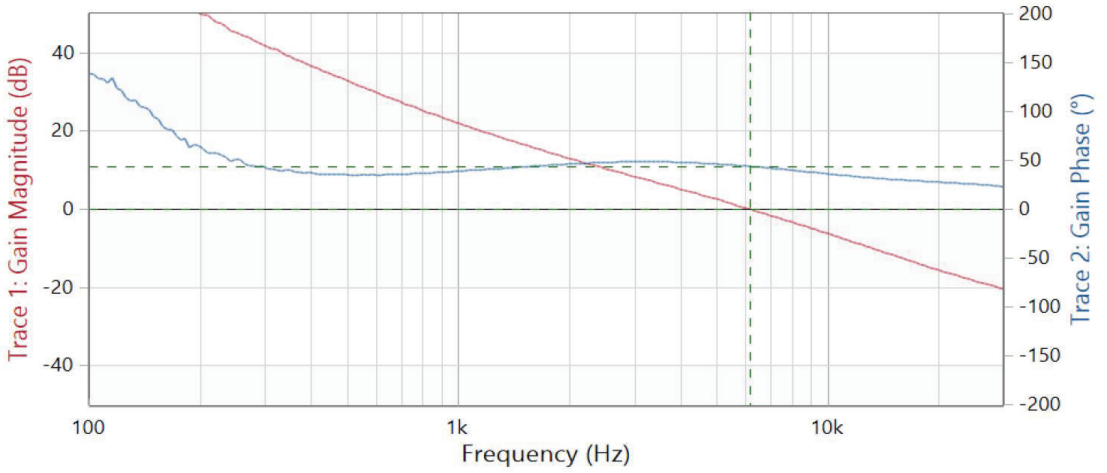

Figure 38 – Initial design with 6.2 kHz bandwidth and 44° phase margin.

Finally, mitigate system noise by avoiding high switching currents through signal ground. Minimize trace lengths between resistor dividers and avoid putting ICs under the transformer since magnetic coupling may cause circuit misbehavior.

IX. Compensating an Isolated Flyback Converter

Compensating an isolated power supply is not as straight-forward as a simple buck regulator. The commonly used TL431 plus optocoupler circuit (powered from the converter output) provides a different response from an op amp error amplifier. Consider our previous example of the 24 V, 36 W flyback shown in Figure 25, which has the loop response shown in Figure 38. The bandwidth is 6.2 kHz and the phase margin is only 44°. How can the phase margin be increased?

Many engineers are tempted to put a resistor in series with C14, hoping to implement a type-2 compensator and introduce a zero into the loop. Those engineers are often perplexed by the results. To get a better understanding of the effects of the components in the TL431 circuit, see what happens when we change one value at a time. Then we will look at the math to understand why.

First, consider what happens when the value of C14 is increased. This capacitor looks like an integrating capacitor, so it may seem that increasing this capacitor will lower the gain curve but preserve the shape of the phase plot. Figure 39 shows how the gain and phase curves change when C14 is increased from 10 nF to 56 nF. The crossover

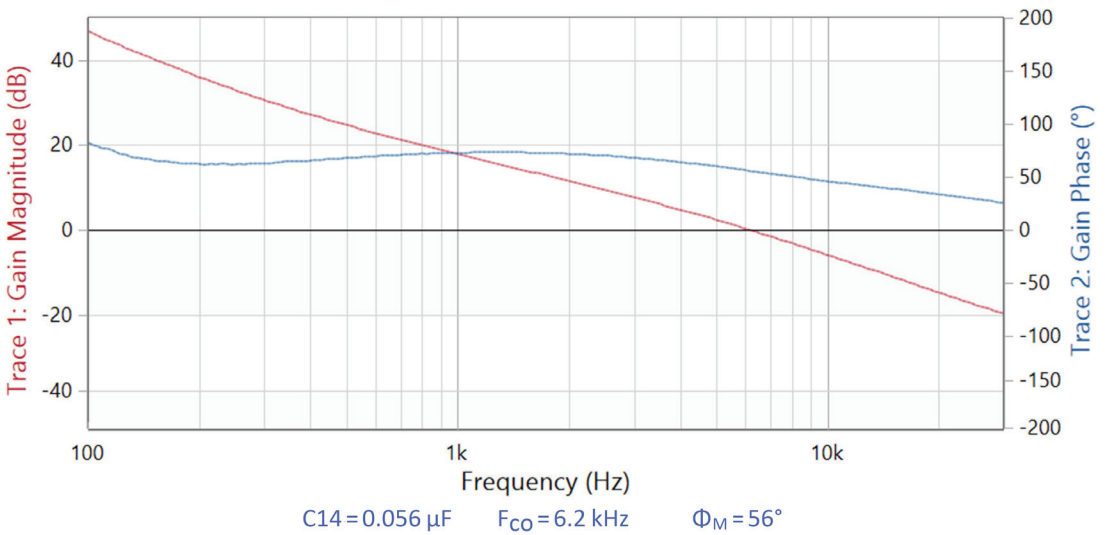

Figure 39 – Increasing C14 increases phase margin but doesn't affect bandwidth.

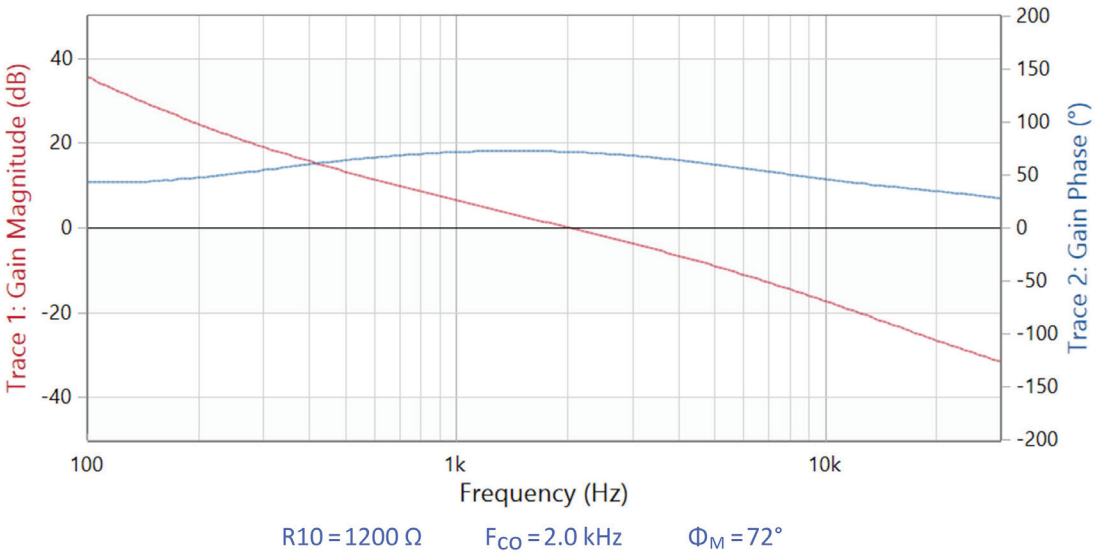

Figure 40 – Increasing R10 lowers the bandwidth.

frequency remains 6.2 kHz, but the phase margin is increased to 56°. Notice that the gain is reduced at lower frequencies, but the shape of the gain curve did not change above 10 kHz. Increasing this capacitor also provides a modest increase in phase above 200 Hz.

Next, consider the effect of changing the value of R10, as shown in Figure 40, where R10 has been increased from 300 Ω to 1200 Ω. Notice that the phase plot didn't change significantly. The magnitude of the gain is reduced by 12 dB across the entire frequency range, but the shape of the gain curve did not change. The crossover frequency is reduced to 2 kHz, and the phase margin is now 72°. The loop now has a large amount of gain and phase margin.

Figure 41 provides a model for analyzing the frequency response of the TL431 optocoupler circuit, where we are interested the small signal gain from V_{OUT} to FEEDBACK. Notice that there are two paths from V_{OUT} to the optocoupler. The outer loop is the one that we are all familiar with in non-isolated supplies. However, perturbations on V_{OUT} also create an inner loop through the pull-up resistor (R1) of the optocoupler. The presence of the inner loop causes the frequency response of this circuit to be drastically different than the outer loop alone [8].

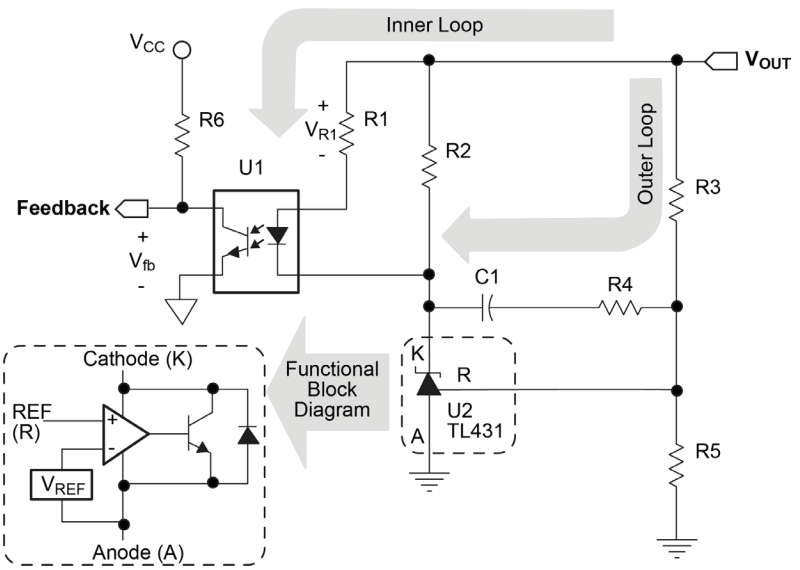

Figure 41 – TL431 and optocoupler feedback circuit has two feedback paths.

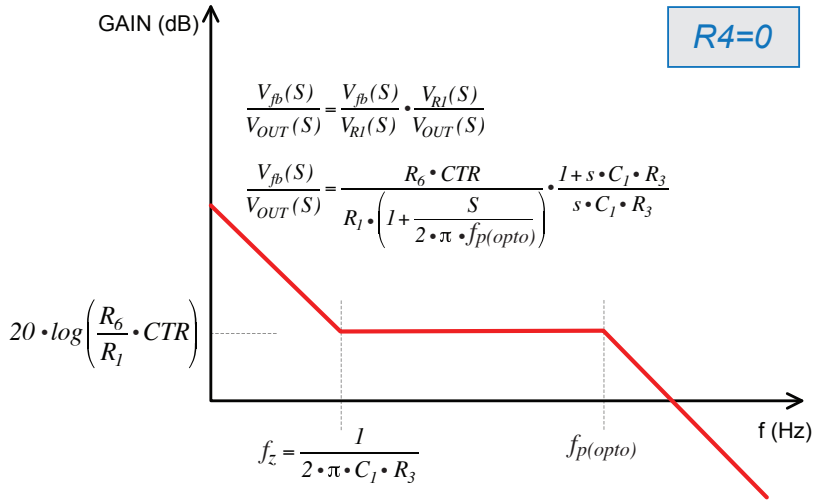

Figure 42 – Gain of TL431 circuit.

Figure 42 shows the equations and plot of the gain for the case where R4 is shorted. The gain is the product of two terms. The first term is the gain from the voltage across R1 to FEEDBACK, which represents the gain of the optocoupler. The gain of this section is determined by R1, R6 and the optocoupler CTR. Changing any of these values will allow us to add or take away gain to the loop, but there are limits to how much gain we can attenuate (remember our previous discussion on current starving the optocoupler). The bandwidth of the optocoupler also introduces a pole into the response.

The second term is the gain from V_{OUT} to the voltage across R1. This term has a pole at the origin and a single zero set by the values of R3 and C1. Notice that the gain of this term goes to 0 dB above the zero frequency. Increasing the value of C1 simply pushes the zero to a lower frequency, which will boost the phase, but does not attenuate the gain. This explains the results seen in our example above.

Now let's see what happens when R4 is introduced. The new equations and gain plot are shown in Figure 43. The response of the first term does not change. The second term still has a pole at the origin, but the location of the zero is now determined by C1 and the sum of R3 and R4. Adding R4 increases the mid-band gain but doesn't introduce an additional zero. In most cases, R4 provides no additional benefit.

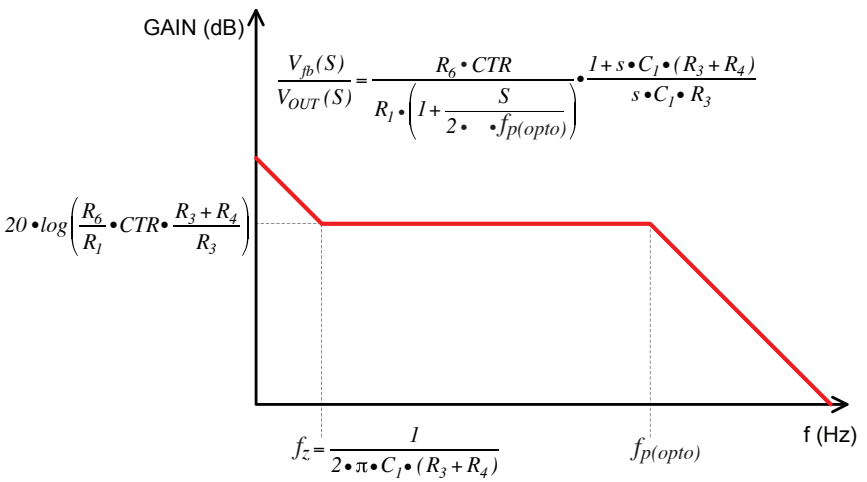

Figure 43 – Introducing R4 increases the mid band gain.

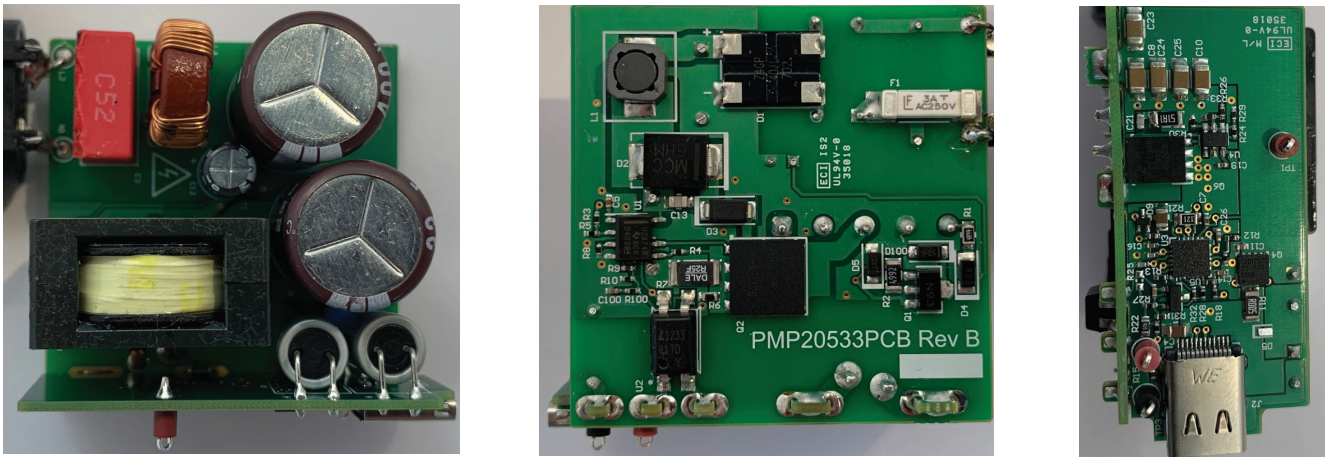

Figure 44 – This 45 W QR flyback creates audible noise, top view (left), bottom view (center), side view (right).

X. Mitigating Audible Noise

When audible noise is not a primary consideration in the design phase of a power supply, it may rudely show up later during the testing phase. Most controllers are designed to operate well above audible frequencies during full load operation. As we discussed earlier, modern controllers reduce the frequency or enter burst modes of operation at lighter loads in order to keep the efficiency high and minimize standby power consumption. At light loads, you may find your power supply operating below 20 kHz and susceptible to generating audible noise.

For example, the 45 W power supply pictured in Figure 44 generates an annoying buzzing sound when supplying a load of 10 W. The noise spectrum measured with a microphone is pictured in Figure 45. Something in the construction of this power supply is transducing electrical energy into acoustical energy. Can you identify the offending component?

Transformers and inductors are common sources for audible noise. Electro-mechanical forces on the wires and magnetic cores can cause movement and displacement of air resulting in perceptible sound. The transformer in this power supply has been glued and vacuum varnished and is not the source of the noise. However, the center drum of the input inductor (L1) is unsecured, as shown in the zoom of Figure 46, and is only held in place by two wires.

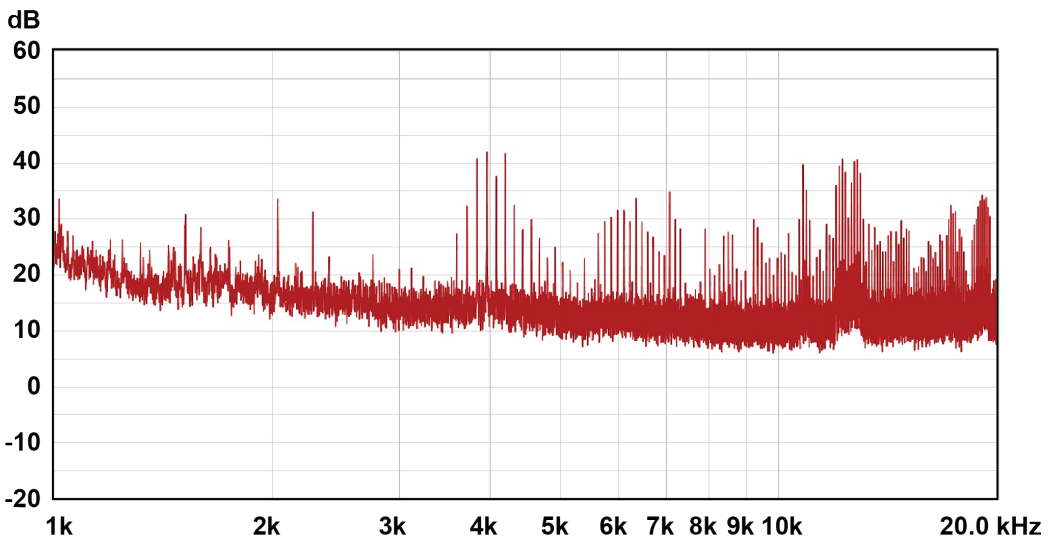

Figure 45 – Measured audible noise.

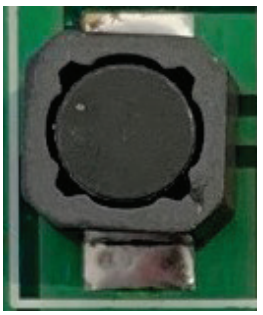

Figure 46 – Unsecured drum core inductors make great speakers.

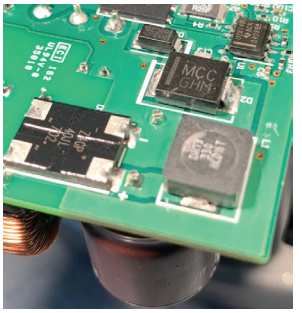

Figure 47 – Inductor with the center drum glued.

When excited with pulsating currents, the center drum acts like a speaker and is the source of the buzzing sound. Replacing this inductor with another inductor that has the center drum glued in place eliminates the noise, as shown in the photo of Figure 47 and new measurements of Figure 48.

that generates the most audible noise. To prevent "singing capacitors" it is best to place capacitors with large ripple current near the edge of the PCB or add a slit in the PCB directly underneath the capacitor. Another technique is to mount two parallel capacitors symmetrically on opposite sides of the PCB so that the forces cancel.

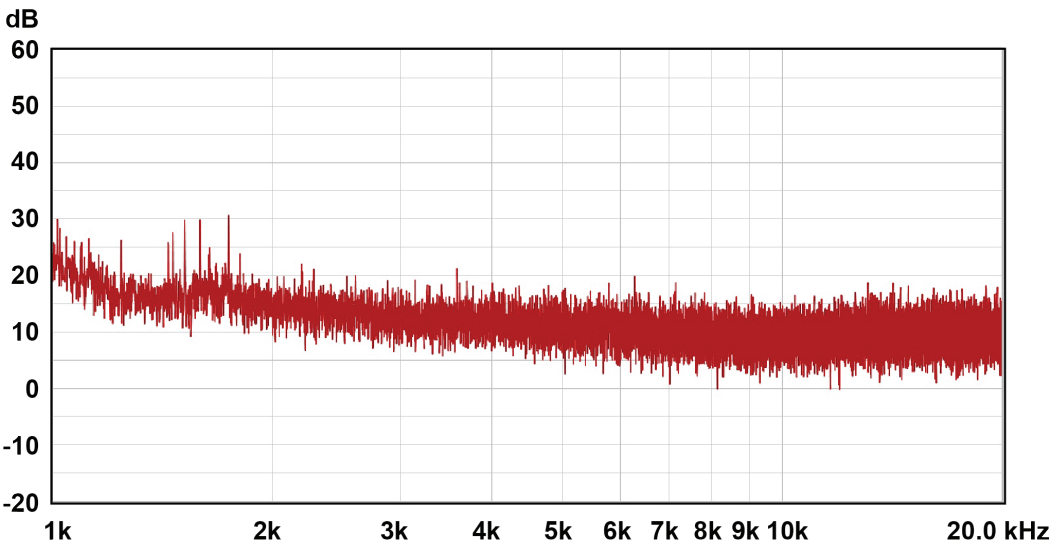

Figure 48 – Audible noise mitigated.

Ceramic capacitors are another common source of audible noise, due to the piezoelectric effect [9, 10]. Essentially when the capacitor is excited by pulsating currents, the ceramic material expands and contracts causing a deformation of the capacitor as shown in Figure 49. The force generated can also cause deformation or flex of the circuit board in the area that the capacitor is mounted. It is often the flex of the circuit board

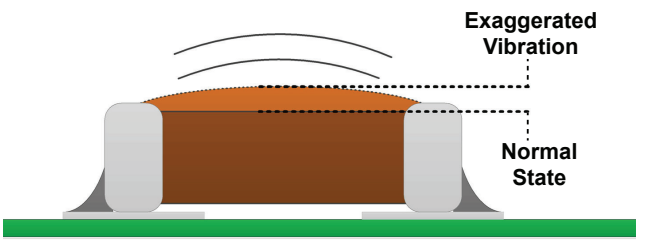

Figure 49 – Piezoelectric effect in ceramic capacitors.

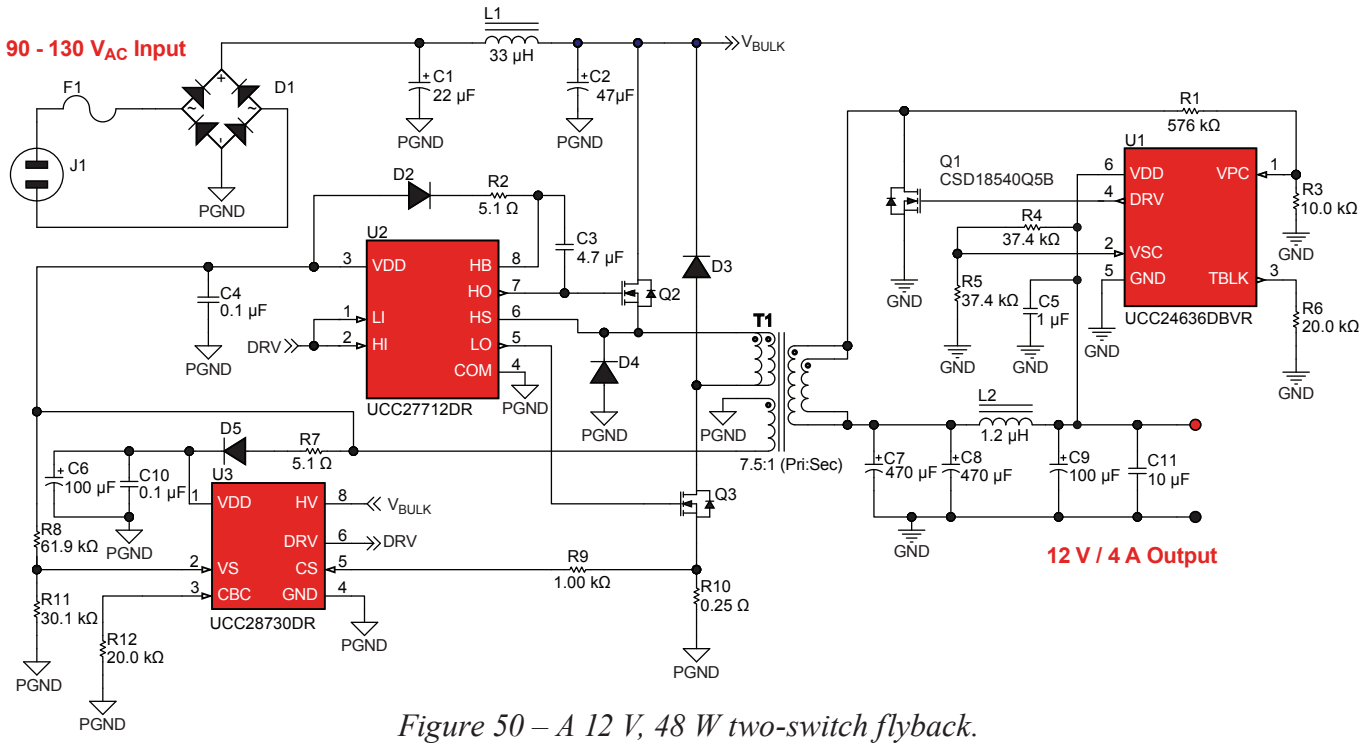

Figure 50 – A 12 V, 48 W two-switch flyback.

XI. Sizing the Input Capacitor

For our final common mistake, consider the 12 V, 48 W two-switch flyback shown in Figure 50. This power converter operates at a nominal input voltage of 115 V_{AC}, but as the input is reduced to around 95 V_{AC}, a mysterious ripple appears on the output voltage. This converter needs to operate at input voltages as low as 90 V_{AC}, 60 Hz, so this problem needs to be resolved. Figure 51 shows a plot of the output ripple voltage and the input voltage after the rectifier, labelled "V_{BULK}" on the schematic. What is the cause of this excessive ripple voltage?

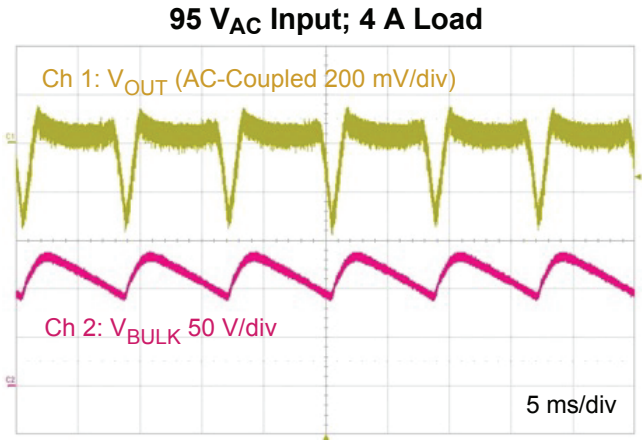

Figure 51 – What is causing the excessive output ripple?

A big clue is the frequency of the ripple. Notice it is 120 Hz and the droops align with the valleys of the rectified AC voltage. When the input voltage sags, the output voltage starts to droop. The problem is due to not enough input capacitance and a limited duty cycle. With only 69 µF after the bridge rectifier, the input voltage sags below 90 V between line cycles which demands over 50% duty cycle. However, the duty cycle of a two-switch flyback is limited to a maximum of 50%, which in turn limits the power delivered to the output during the valleys of the rectified AC voltage.

Increasing the amount of bulk input capacitor reduces the sag on the rectified AC voltage, as shown in Figure 52. With a total of 136 µF, the supply can operate down to an input voltage of 90 V_{AC}, 60 Hz, with no noticeable 120 Hz ripple on the output. This keeps the minimum rectified AC voltage above 100 V. Alternatively, the turn ratio of the transformer can also be adjusted to keep the duty below 50% at lower input voltages.

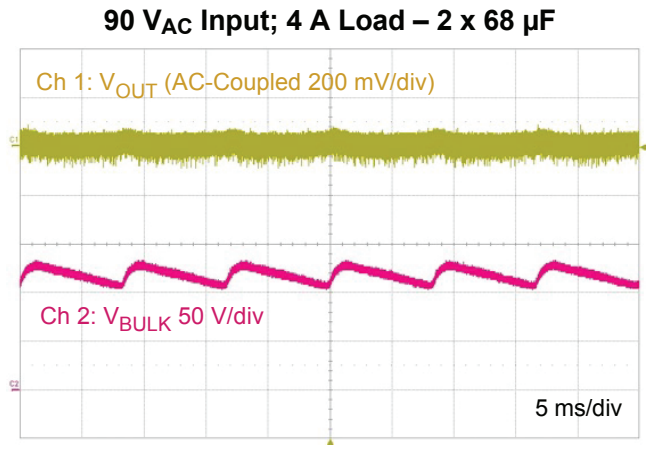

Figure 52 – Increased bulk capacitance.

The bulk input capacitors are often the largest components in a power supply. It is obviously desirable to minimize the amount of capacitance to reduce the size. The chart of Figure 53 shows the amount of capacitance needed to keep the rectified voltage from sagging below 80 V with a 90 V_{AC}, 50 Hz input. A good simple rule to follow is to have at least 1.5 µF/W of bulk capacitance to support your minimum input voltage requirements.

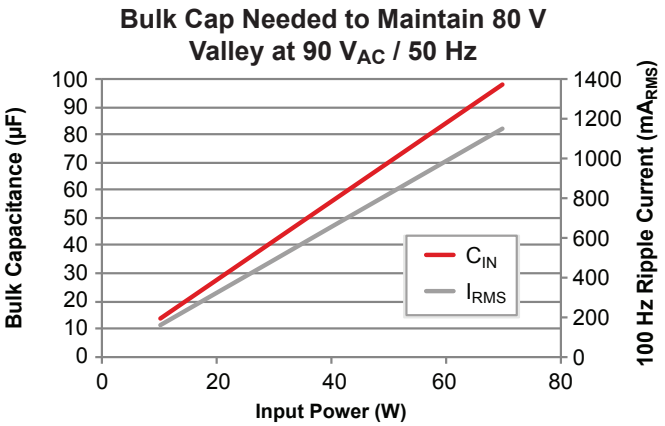

Figure 53 – Typical bulk capacitor requirements.

Also shown in Figure 53 is the 100 Hz ripple current in the capacitor versus power. Care needs to be taken not to exceed the ripple current rating of the capacitor. The bulk capacitor needs to be sized for not just the ripple current at twice the line frequency, but also the ripple current created by the power supply at the switching frequency.

Aluminum electrolytic capacitors are usually the least reliable component in the power supply. The lifetime of the capacitors typically determines the life of the product. Arrhenius' law states that the capacitor life doubles for every 10ºC decrease in temperature. The stated life, such as 2000 hours, assumes operation at rated temperature and ripple current. Designing for low failure rates is possible by using capacitors rated well above their maximum operating temperature and ripple current.

XII. Summary

There is a consistent theme under riding each of the examples that we looked at. In each case, the problem can only be solved if the right information is examined. Gathering and evaluating data is critical for fast debugging of any problem. This is true in power supply design, just as it is true in life.

For startup issues, monitoring the output voltage, V_{DD} voltage and switched node often reveals the source of the problem. For fault protection, study the controller data sheet to identify all possible shutdown mechanisms, and then monitor the IC waveforms for each. Carefully study the characteristics of the optocoupler and make sure it is properly biased for temperature, initial tolerance and life. Consider the turn-on threshold of FETs, especially in SR applications with lower output voltages, to ensure they are fully enhanced. Use a higher clamping voltage to minimize loss and improve efficiency. Minimizing loss in startup circuits and operating at lower frequencies (or burst mode) is critical to reducing standby power consumption. Understanding the causes and effects of parasitic elements are key to a successful power converter layout. The two feedback paths of the optocoupler and TL431 alter the feedback gain equations, compared to common non-isolated supplies, and knowing how each component affects the gain and phase allows quick modification of the feedback. For audible noise, look for unsecured magnetic components and ceramic capacitors for your initial suspects.

Finally, avoid issues at minimum AC input by providing sufficient bulk input capacitance.

Often, we gain the most knowledge from our mistakes. With power supply design, there is plenty of opportunity to learn! Hopefully, the information provided in this paper will allow you to learn from the mistakes of others.

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