High-Frequency Quasi-Resonant Converter Technologies

FRED C. LEE, SENIOR MEMBER, IEEE

Invited Paper

Resonant switch topologies operating under the principle of zero-current switching (ZCS) and zero-voltage switching (ZVS) are introduced to minimize switching losses, stresses, and noises. Employing the resonant switch concept, a host of new quasi-resonant converters (QRCs) are derived from the conventional PWM converters. They are capable of operating in megahertz range, with a significant improvement in performance and power density. Performances of ZCS- and ZVS-QRCs are analyzed and compared. Design of power stages, gate drives, and feedback controls are discussed.

I. INTRODUCTION

Electronic power processing technology has evolved around two fundamentally different circuit schemes: duty-cycle modulation, commonly known as Pulse-Width Modulation (PWM), and resonance. The PWM technique processes power by interrupting the power flow and controlling the duty cycle, thus, resulting in pulsating current and voltage. The resonant technique processes power in a sinusoidal form. The power switches are often commutated under zero-current ("*soft*" turn-off) but switches are turned on with an abrupt increase of device current ("*hard*" turn-on). In cases where resonant converters operate above the resonant frequency, the switches are turned off abruptly (forced or hard turn-off) but turned on softly. Compared with PWM converters, the switching losses and stresses of resonant converters are reduced; however, the conduction loss is generally increased since the sinusoidal current produces higher rms current. Due to circuit simplicity and ease of control, the PWM technique has been used predominantly in today's power electronics industry, particularly, in low-power applications. Resonant technology, although well-established in high-power SCR motor drives and uninterrupted power supplies, has not been widely used in low-power dc-dc converter applications due to its circuit complexity.

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The author is with the Virginia Power Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA 24061, USA.

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With available devices and circuit technologies, PWM converters have been designed to operate generally with a 30–50-kHz switching frequency. In this frequency range, the equipment is deemed optimal in weight, size, efficiency, reliability, and cost. In certain applications where high-power density is of primary concern, the conversion frequency has been chosen as high as several hundred kilohertz. With the advent of power MOSFETs, device switching speeds of tens of megahertz are now possible. Accompanying the higher switching frequency are increased switching stresses and losses. Furthermore, the presence of leakage inductances in the transformer and junction capacitances in the semiconductor devices causes the power devices to inductively turn-off and capacitively turn-on. As the semiconductor device switches off an inductive load, voltage spikes induced by the sharp *di/dt* across the leakge inductances produce increased voltage stress and noise.

On the other hand, when the switch turns on at a high voltage level, the energy stored in the device's output capacitance, $0.5CV^2$, is dissipated internally when the device is switched on. Furthermore, turn-on at high voltage levels induces a severe switching noise through the Miller capacitor coupled into the drive circuit, which leads to significant noise and instability in the drive circuit. The detrimental effects of parasitic elements become more pronounced as the switching frequency is increased.

To improve switching behavior of semiconductor devices in power processing circuits, two techniques were proposed. The first is the **zero-current-switching** (ZCS) technique. The concept of resonant switches was introduced [1]–[7]. By incorporating an *LC* resonant circuit, the current waveform of the switching device is forced to oscillate in a quasi-sinusoidal manner, therefore, creating zero-current-switching conditions during both turn-on and turn-off. By simply replacing the power switch(es) in PWM converters with the proposed resonant switch, a family of quasi-resonant converters (QRCs) has been derived. This new family of circuits can be viewed as a hybrid of PWM and resonant converters. QRCs utilize the principle of inductive or capacitive energy storage and transfer in a manner similar to PWM converters, and their circuit topologies also resemble those of PWM converters. However, an *LC* tank

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circuit is always present near the power switch and is used not only to shape the current and voltage waveforms of the power switch but, also, to store and transfer energy from the input to the output in a manner similar to the conventional resonant converters. For off-line as well as dc-dc converter applications, the zero-current-switching technique is very effective up to 1–2 MHz, since it can eliminate turn-off switching loss and switching stresses. Employing the zero-current switching technique, several off-line converter topologies have been successfully implemented achieving a power density of 25 W/in^3 [8]–[10]. However, to operate the semiconductor switches above one megahertz, the capacitive turn-on loss associated with the discharging of energy stored in the parasitic junction capacitance of the MOSFET becomes the primary limiting factor.

The second technique proposed is **zero-voltage-switching** (ZVS) [1], [11]. By using an *LC* resonant network, the voltage waveform of the switching device can be shaped into a quasi-sine wave, such that zero-voltage conduction is created for the switch to turn on and turn off without incurring any switching loss. This technique eliminates the turn-on loss associated with the parasitic junction capacitances. Practical quasi-resonant-converter circuits operating in frequencies over 10 MHz have been implemented [12]–[16].

The fundamental characteristics of the zero-current and zero-voltage-switching techniques and the basic structure of the zero-voltage-switched circuit are discussed in this paper. Through the establishment of the zero-current switching technique and the proposed basic circuit structures, a large family of ZCS-QRCs have been derived. Similarly, the zero-voltage switching technique has led to the discovery of a large family of ZVS-QRCs. Furthermore, the duality relationship which exists between the zero-current-switching and the zero-voltage-switching techniques is established. The recognition of the duality relationship between these two techniques provides a framework permitting knowledge transfer from one converter family to the other.

In Section II, the concepts of the ZC resonant switch and ZV resonant switch are discussed. Employing the resonant switch concept, a class of QRCs are generated and some basic topologies are presented.

Similarly, ZVS-QRCs are discussed in Section IV. The duality relationship between the ZCS-QRF family and ZVS-QRC families is presented in Section V, with a comparison of merits and disadvantages of the two families of QRCs. Issues related to gate-drive circuit design and closed-loop controls for QRCs are discussed in Sections VI and VII, respectively. Performance of breadboarded flyback ZVS- and ZCS-QRCs are presented in Section VIII.

II. Quasi-Resonant Converters

A. Resonant Switches

A resonant switch represents a subcircuit consisting of semiconductor switch S_1 and resonant elements L_r and C_r. For a ZC resonant switch, as shown in Fig. 1(a), inductor L_r is in series with switch S_1 to achieve zero-current switching; in a ZV resonant switch, as shown in Fig. 1(b), capacitor C_r is in parallel with switch S_1 to achieve zero-voltage switching.

1) ZC Resonant Switches [2]: If the ideal switch S_1 is implemented by a unidirectional switch in Fig. 2(a); the resonant switch is confined to operate in a **half-wave mode,** in the sense that the switch current is permitted to resonate only in the positive half cycle. On the other hand, if diode D_1 is connected in antiparallel with Q_1 as shown in Fig. 2(b), the switch current can flow bidirectionally and the resonant switch now operates in **full-wave mode.**

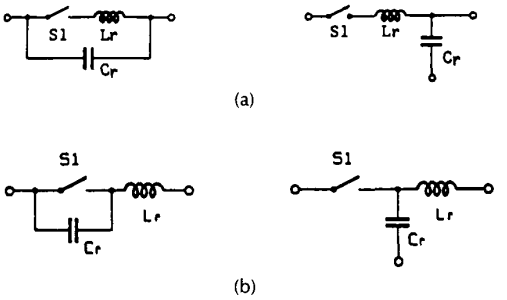

Fig. 1. (a) ZC resonant switches. (b) ZV resonant switches.

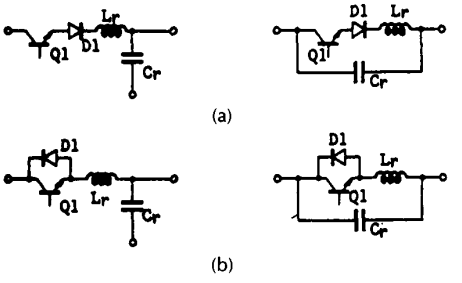

Fig. 2. Current-mode resonant switch configurations. (a) Half-wave configurations. (b) Full-wave configurations.

In essence, the resonant *LC* circuit is used to shape the current waveform through switch S_1. At turn-on, the device voltage (V_{CE} or V_{DS}) can be driven into saturation before the current slowly rises. Because of the resonance between L_r and C_r, current through switch S_1 will oscillate, thus, allowing switch S_1 to be naturally commutated.

The load-line trajectory of PWM switching behavior, shown as trajectory *A* in Fig. 3, traverses across the high-stress region in which the device is subjected to simultaneous high voltage and high current; whereas the load-line trajectory of a resonant switch, shown as trajectory *B*, moves along the axes. Since no simultaneous high voltage and high current are exerted on the switch device, the switching stresses and losses are minimal.

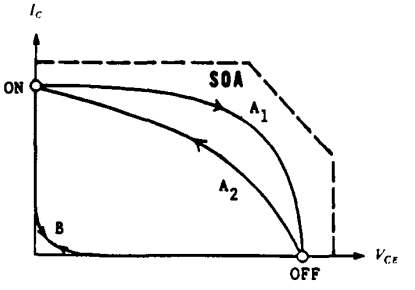

Fig. 3. Switching load line trajectory. (a) Conventional PWM switching. (b) ZC resonant switching.

2) ZV Resonant Switches [9]: As in the case of a ZC resonant switch, the structure of S_1 determines the operation mode of the ZV resonant switch. If ideal switch S_1 is implemented by a transistor Q_1 and an antiparallel diode D_1, as shown in Fig. 4(a), the voltage across capacitor C_r is clamped by D_1 at zero during the negative half of the resonant cycle. The resonant switch is operating in half-wave mode. On the other hand, if S_1 is implemented by Q_1 in series with D_1, as shown in Fig. 4(b), and the voltage across C_r can oscillate freely, then the resonant switch is operating in a full-wave mode.

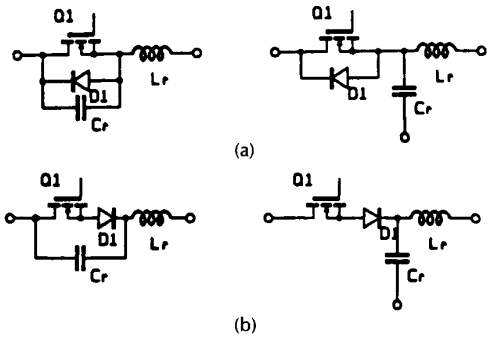

Fig. 4. Voltage-mode resonant switches. (a) Half-wave mode implementation. (b) Full-wave mode implementation.

B. A New Family of Quasi-Resonant Converters

The concept of a resonant switch can be directly applied to a large number of conventional PWM converters. Simply replacing the power switch(es) of a PWM converter with the ZC resonant switch, a new family of ZCS-QRCs can be derived. Some basic topologies are illustrated in Fig. 5.

Similarly, a family of ZVS-QRCs can be derived. A few topological variations of the ZVS-QRCs are shown in Fig. 6. Notice that in the isolated version of a quasi-resonant converter, the leakage inductances of the transformer can be utilized as the resonant inductor. Moreover, when the junction capacitance of the switching device is used as the resonant capacitor, in the case of ZVS, the number of circuit components are further reduced.

A particularly interesting topology is the flyback ZVS-QRCs of Fig. 6(e). When the leakage inductance of the transformer and the junction capacitance of the switching device are used as the resonant elements, the converter contains the fewest components and still achieves the zero-voltage switching property.

Many topological variations of QRCs can be derived using

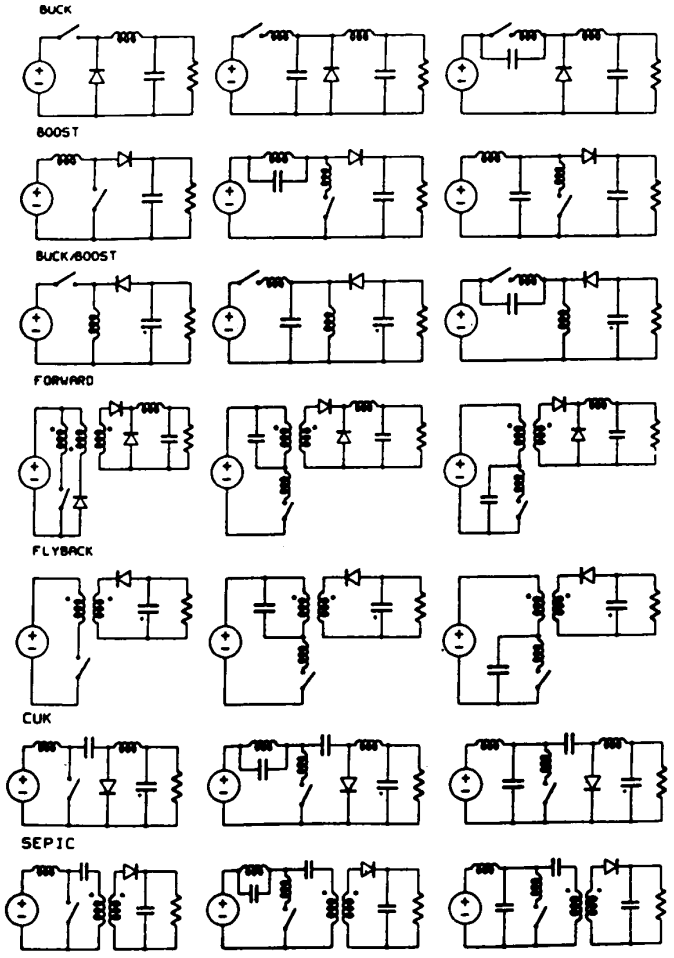

Fig. 5. A family of ZCS-QRCs.

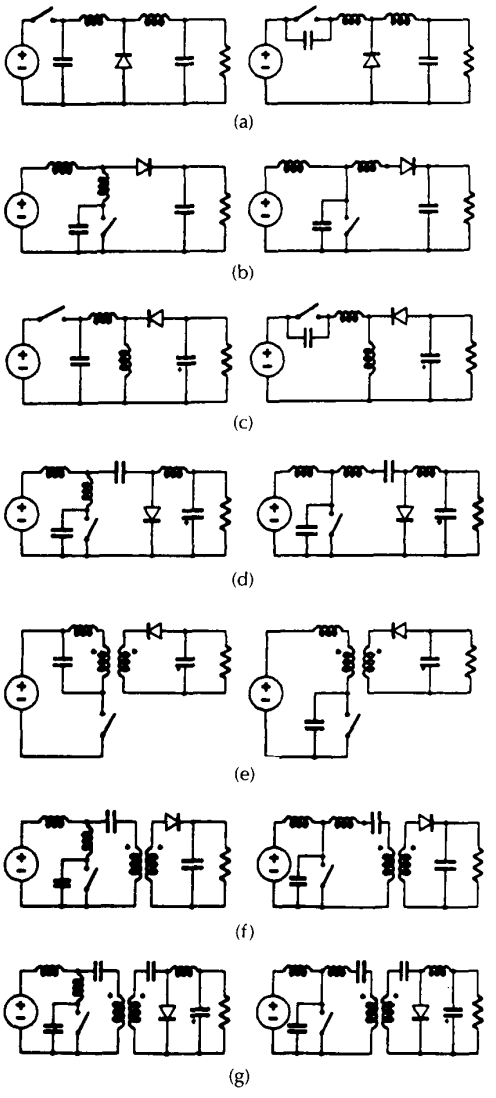

Fig. 6. A family of ZVS-QRCs. (a) Buck converter. (b) Boost converter. (c) Buck/boost converter. (d) Cuk converter. (e) Flyback converter. (f) SEPIC converter. (g) Isolated cuk converter.

the basic concept of ZC and ZV resonant switches described above. They were presented in [17]–[19].

III. Zero-Current-Switched Quasi-Resonant Converters (ZCS-QRCs)

A. Principle of Operation [3]

A buck quasi-resonant converter, as shown in Fig. 7(a), is employed to describe the principle of operation. To analyze the steady-state circuit behavior, the following assumptions are made:

- $L_0 \gg L_r$.
- Output filter $L_0 - C_0$ and the load are treated as a constant current sink.
- Semiconductor switches are ideal, i.e., no forward voltage drop in the on-state, no leakage current in the off-state, and no time delay at both turn-on and turn-off.
- Reactive elements of the tank circuit are ideal.

The following variables are defined:

- Characteristics impedance $Z_n \equiv \sqrt{L_r/C_r}$.
- Resonant angular frequency $\omega \equiv 1/\sqrt{L_rC_r}$.
- Resonant frequency $fn \equiv \omega/2\pi$.

A switching cycle can be divided into four stages; their equivalent circuits are shown in Fig. 7. Suppose that before S_1 is turned on, diode D_0 carries the output current I_0, and resonant capacitor voltage Vc_r is clamped at zero. At the beginning of a switching cycle, $t = T_0$, S_1 is switched on.

1) Inductor Charging Stage [T_0, T_1] (Fig. 7(b)): Input current I_l rises linearly, and is governed by the state equation

$$L_r(di_l/dt) = V_l. \tag{1a}$$

The duration of this stage, $Td_1(=T_1 - T_0)$, can be solved with boundary conditions $I_l(0) = 0$ and $I_l(Td_1) = I_0$. Thus

$$Td_1 = L_TI_0/V_l. \tag{1b}$$

2) Resonant Stage [T_1, T_2] (Fig. 7(c)): At time T_1 when the input current rises to the level of I_0, D_0 is commutated off, and the amount of current $i_l(t) - I_0$ is now charging Vc_r as can be seen from Fig. 7(c).

The state equations are

$$C_r(dVc_r/dt) = i_l(t) - I_0 \tag{2a}$$

$$L_r(dI_l/dt) = V_l - Vc_r(t) \tag{2b}$$

with the initial conditions

$$Vc_r(0) = 0 \quad \text{and} \quad I_l(0) = I_0. \tag{2c}$$

Therefore

$$i_l(t) = I_0 + (V_l/Z_n) \sin \omega t \tag{2d}$$

$$Vc_r(t) = V_l(1 - \cos \omega t). \tag{2e}$$

If a half-wave resonant switch is used, switch Q_1 will be naturally commutated at time T_a when the resonating input current $i_r(t)$ reduces to zero, as shown in Fig. 8(a). On the other hand, if a full-wave resonant switch is used, current $i_l(t)$ will continue to oscillate and feed energy back to source V_l through the antiparallel diode D_1, as shown in Fig. 8(b). Current through D_1 again oscillates to zero at time T_b. The duration of this stage, $Td_2(=T_2 - T_1)$, can be solved from (2d) by setting $i_l(Td_2) = 0$. Thus

$$Td_2 = \alpha/\omega \quad \text{where} \quad \alpha = \sin^{-1}(-Z_nI_0/V_l)$$

$$\pi \le \alpha \le 3\pi/2 \quad \text{and} \quad T_2 = T_a \quad \text{for half-wave mode}$$

$$3\pi/2 \le \alpha \le 2\pi \quad \text{and} \quad T_2 = T_b \quad \text{for full-wave mode.} \tag{2f}$$

At time T_2, $Vc_r = Vcb$, can be solved from (2e):

$$Vc_r(Td_2) \equiv Vcb = V_l(1 - \cos \alpha). \tag{2g}$$

3) Capacitor Discharging Stage [T_2, T_3] (Fig. 7(d)): Since switch S_1 is off at time T_2, C_r begins to discharge through the output loop and Vc_r drops linearly to zero at time T_3, as shown in Fig. 8(a) and (b). The state equation during this interval is

$$C_r(dVc_r/dt) = I_0. \tag{3a}$$

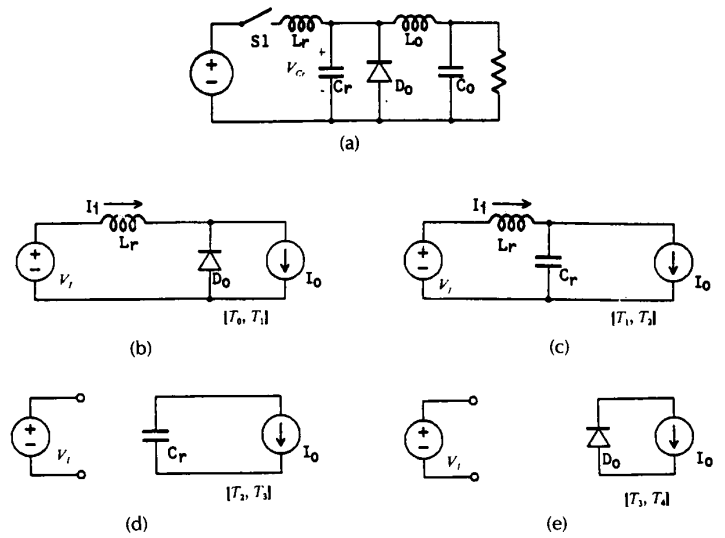

Fig. 7. Buck quasi-resonant (a) converter and its equivalent circuits during four stages of a switching cycle. (b) Inductor charging stage, $[T_0, T_1]$. (c) Resonant stage, $[T_1, T_2]$. (d) Capacitor-discharging stage, $[T_2, T_3]$. (e) Free-wheeling stage, $[T_3, T_4]$.

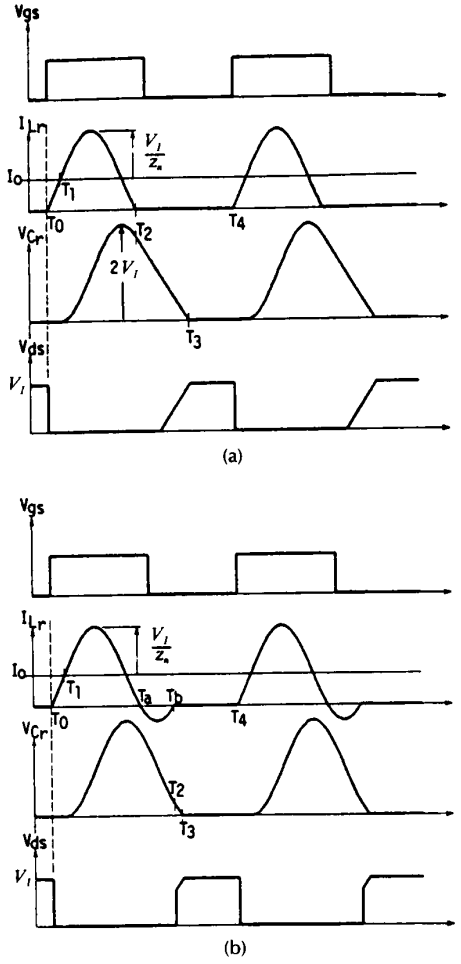

Fig. 8. Waveforms of the buck resonant converter. (a) Half-wave mode. (b) Full-wave mode.

The duration of this stage, $Td_3(=T_3 - T_2)$, can be solved with the initial condition $Vc_r(0) = Vcb$

$$Td_3 = C_r Vcb/I_0 = C_r V_I(1 - \cos\alpha)/I_0. \tag{3b}$$

4) Free-wheeling Stage [T_3, T_4] (Fig. 7(e)): Output current flows through diode D_0. The duration of this stage is $Td_4(=T_4 - T_3)$, and

$$Td_4 = T_s - Td_1 - Td_2 - Td_3 \tag{4}$$

where T_s is the period of a switching cycle.

Typical circuit waveforms, as shown in Fig. 8(a) and (b), clearly demonstrate the zero-current switching property.

B. DC Voltage-Conversion Ratio

Output voltage V_0 can be solved by equating input energy per cycle E_i and output energy per cycle E_0.

Where

$$E_i = V_I\left[\int_{T_0}^{T_1} i_I(t)\,dt + \int_{T_1}^{T_2} i_I(t)\,dt\right] \tag{5}$$

and

$$E_0 = V_0 I_0 T_s. \tag{6}$$

From (1b), (2d), and (3b)

$$V_0 = V_I(Td_1/2 + Td_2 + Td_3)/T_s. \tag{7}$$

Given I_0 and T_s values, Td_1, Td_2, and Td_3 can be solved from (1b), (2a)–(2g), and (3b). Output voltage V_0 can be solved from (7).

By defining $x \equiv V_0/V_I$, and $r \equiv R/Zn$, (7) can be written as

$$x - (1/2\pi)(fs/fn)[(x/2r) + \sin^{-1}(-x/r) + (r/x)(1 + \text{sign}\sqrt{1 - (x/r)^2})] = 0. \tag{8}$$

Define

$$\sin^{-1}(-x/r) \equiv \alpha$$

then

for half-wave mode

$$\pi < \alpha < 3\pi/2 \qquad \text{sign} = +1$$

for full-wave mode

$$3\pi/2 < \alpha < 2\pi \qquad \text{sign} = -1.$$

Voltage-conversion ratios for the buck resonant converter are plotted in Fig. 9(a) and (b) for the half-wave mode and full-wave mode, respectively. It can be seen that the voltage-conversion ratio in the half-wave mode is very sensitive to load variation, while in the full-wave mode the voltage-conversion ratio is almost independent of load variation. This can be understood by examining the (measured of simulated) waveforms of i_l and Vc_r in Fig. 10. Under heavy load, i_l is offset by a large amount of I_0, and the negative portion of the resonant inductor current, which is the current flowing through the antiparallel diode, is small. When the load is light, i_l is offset by a small amount of I_0 and the reverse current through D_1 is increased. This behavior can be simply stated in the following: as the power switch is turned on, energy is transferred from the source to the resonant tank. When the load demand is light, a large portion of the tank energy is returned to the source. When the load is heavy, most of the tank energy is transferred to the load and only a small portion of that tank energy is returned to the source. Consequently, the antiparallel diode regulates the tank energy such that the voltage-conversion ratio remains constant as the load is varying. For the half-wave mode, the excessive tank energy cannot be returned to the source when the load channel is reduced. Consequently, the operating frequency has to be reduced to regulate the output voltage. A more rigorous discussion of this is given in [3].

It should be noted that the characteristic shown in Fig.

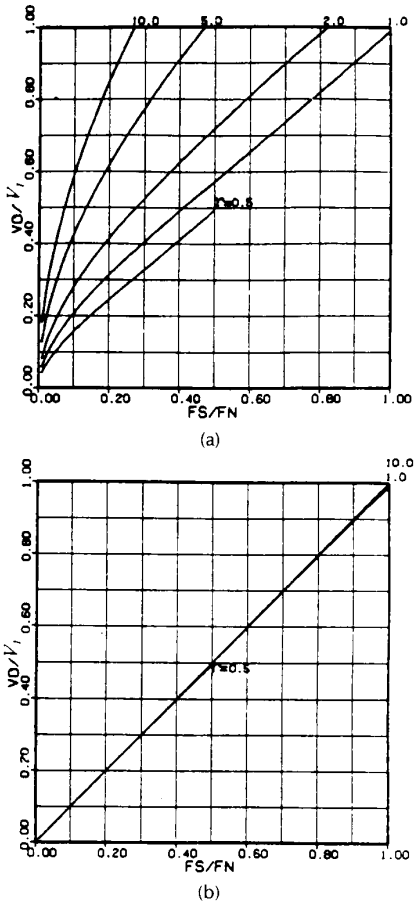

Fig. 9. DC voltage-conversion ratio for the buck resonant converter. (a) Half-wave mode. (b) Full-wave mode.

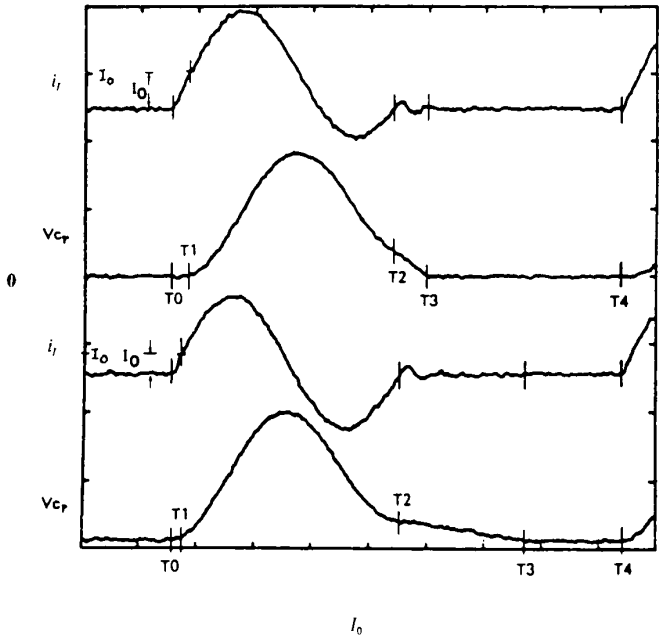

Fig. 10. Waveforms of the buck resonant converter. Upper waveforms: heavy load. Lower waveforms: light load.

9(b) is exactly the same as that of the PWM buck converter provided that the horizontal axis is replaced by the duty-cycle ratio. This conclusion can be extended to other converter topologies as well. This simply implies that the QRCs operating in full-wave mode have the same dc conversion characteristics and small-signal transfer function [20] as their PWM counterparts, while capable of achieving zero-current turn-on and zero-current turn-off.

An examination of the input current waveform i_l of Fig. 10 reveals that i_l contains a dc component of I_0 and an ac component of Vs/Z_n. The ac component is fixed for a given input and characteristic impedance Z_n, and the dc component I_0 is simply the load. To maintain an ac component greater than the dc component, an upper bound exists on the load current above which the zero-current switching property will be lost

$$I_0 \leq V_s/Z_n.$$

IV. Zero-Voltage-Switched Quasi-Resonant Converters (ZVS-QRCs)

One of the fundamental limitations of ZCS-QRCs for very high-frequency operation is the problem of capacitive turn-on loss, whereas this technology is free of turn-off switching losses. The energy stored in the device's output capacitance, $0.5CV^2$, during the off-state is dissipated inside the device when the device is switched on. At high input voltage the capacitive turn-on loss is significant and the dv/dt during turn-on further introduces a severe switching noise through the Miller capacitor which is coupled into the drive circuit.

While not severe in lower switching frequencies, the capacitive turn-on loss becomes the dominating factor when the switching frequency is raised to the megahertz range. For example, a junction capacitance of 100 pF, switching at 300 V, will induce a turn-on loss of 4.5 W at 1 MHz, and 22.5 W at 5 MHz.

The zero-voltage switching technology is proposed to alleviate the losses during turn-on, thus enabling the quasi-resonant converters to operate at a much higher frequency.

A. Principle of Operation

A boost ZVS-QRC is used, as shown in Fig. 11, to illustrate circuit operation [11]. For simplicity, the converter is treated as a constant current source I_l, suppling power to a constant voltage sink V_0.

In steady-state operation, a complete switching cycle can be divided into four stages starting from the moment S_1 turns off. Suppose, before S_1 is turned off, it carries the input current, I_l. Diode D_0 is off and no current is flowing into the voltage load V_0. At time T_0, S_1 turns off, input current I_l is diverted into capacitor C_r. The following description summarizes the circuit operation during each of the four stages.

1) Capacitor Charging Stage [T_0, T_1]: S_1 turns off at T_0. Current I_l flows into C_r; the voltage across C_r, V_{Cr}, rises linearly. At time T_1, V_{Cr} reaches V_0 and diode D_0 conducts. The equivalent circuit of this stage is shown in Fig. 11(b).

2) Resonant Stage [T_1, T_2]: D_0 turns on at T_1, a portion of I_l starts to flow into V_0.

In the half-wave mode of operation, when V_{Cr} drops to zero at T_a (Fig. 12(a)) it is clamped at the zero value by the antiparallel diode D_1 which carries the reverse current. While in full-wave mode, V_{Cr} continues to oscillate to a negative value and return to zero at time T_b. For half-wave mode, the end of this stage, T_2, is equal to T_a; for full-wave mode, it is equal to T_b. The equivalent circuit of this stage is shown in Fig. 11(c). The waveforms for half-wave mode and full-wave mode can be seen in Figs. 12(a) and 12(b), respectively.

3) Inductor Discharging State [T_2, T_3]: After T_2, current i_{Lr} drops linearly and reaches zero at time T_3. The equivalent circuit of this stage is shown in Fig. 11(d).

Normally, in the half-wave mode of operation, transistor Q_1 shall turn on after V_{Cr} drops to zero at T_a and before the current through D_1 drops to zero at T_c. Otherwise, V_{Cr} will begin to recharge and Q_1 will lose the opportunity to turn on under the zero-voltage condition. In the full-wave mode of operation, Q_1 shall turn on between T_a and T_b, when diode D_1 is blocking the negative voltage.

4) Free-Wheeling Stage [T_3, T_4]: At T_3, the entire input current i_l flows through Q_1. I_{Q1} remains constant until Q_1 turns off at T_4. Detailed analysis of the circuit is presented in [11].

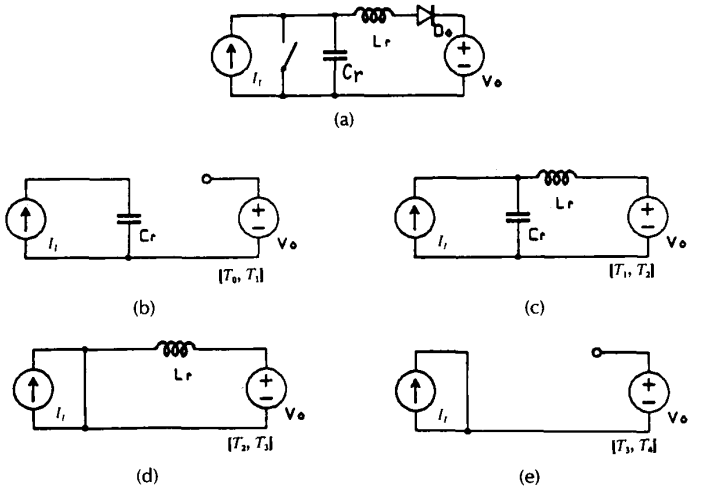

Fig. 11. Simplified circuit for boost ZVS-QRCs (a) and its equivalent circuits during the four stages of a switching cycle. (b) Capacitor charging stage, [T_0, T_1]. (c) Resonant stage, [T_1, T_2]. (d) Inductor-discharging stage, [T_2, T_3]. (e) Input charging stage, [T_3, T_4].

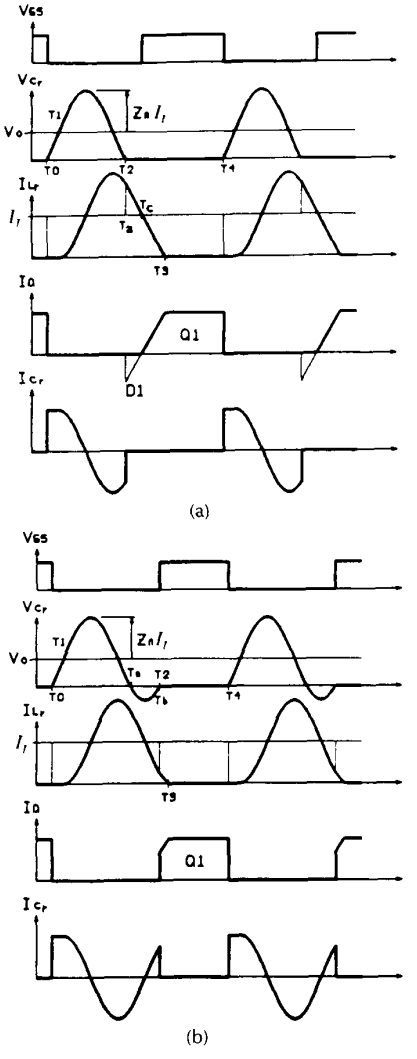

Fig. 12. Typical circuit waveforms of the voltage-mode quasi-resonant boost converter in (a) half-wave mode and (b) full-wave mode.

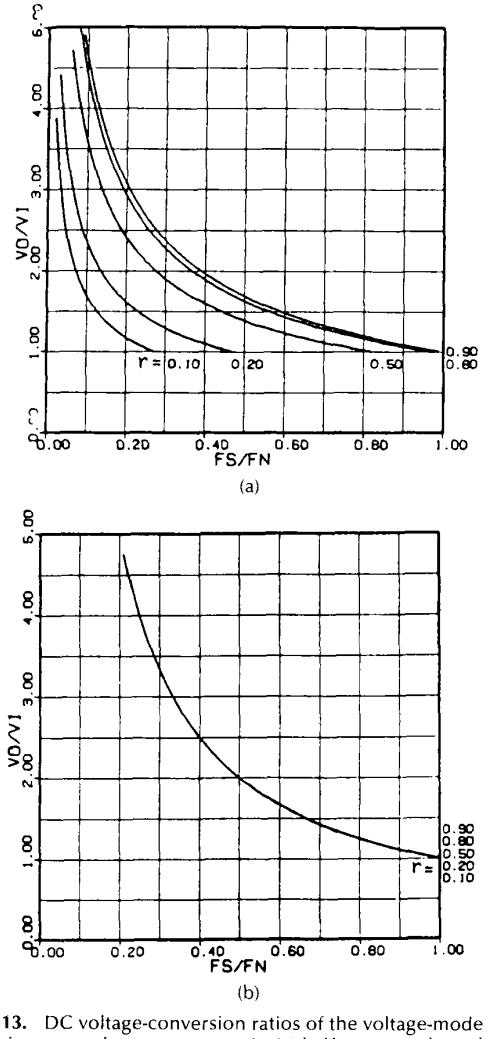

Fig. 13. DC voltage-conversion ratios of the voltage-mode quasi-resonant boost converter in (a) half-wave mode and (b) full-wave mode.

Notice that the voltage waveform of V_{Cr} contains a dc component of V_0 and an ac component of $Z_n i_l$. Since i_l is in proportion to the load current when V_0 and V_l are fixed, the peak value of V_{Cr} increases as the load current is increased. Furthermore, to maintain a larger ac component than dc component, a lower bound on load current exists below which the zero-voltage switching property will be lost. The waveform of the current through Q_1 is somewhat square, and its peak value is the same as that of i_l. This results in a lower rms value of the switch current and the conduction loss is kept minimal.

B. DC Voltage-Conversion Ratio

The dc voltage-conversion ratio, V_0/V_l, as a function of load resistance and switching frequency, can be derived as discussed in Section III-B. The conversion ratio for the boost ZVS-QRC is plotted in Fig. 13(a) and (b) for half-wave mode and full-wave mode, respectively. It can be seen that the voltage-conversion ratio in full-wave mode is insensitive to load variation and is certainly more desirable. However, for full-wave mode, as shown in Fig. 4(b), a series diode is required to provide a reverse-voltage blocking capability. Consequently, the energy stored in the junction capacitances of the semiconductor switch is trapped during off-time and is dissipated internally after the switch turns on. Therefore, full-wave mode suffers from capacitive turn-on losses and *dv/dt* noise, as are ZCS-QRCs, and is not practical for very high-frequency operation.

V. Comparison of ZCS-QRC and ZVS-QRC

A. Duality Relationship

It has been shown that a duality relationship exists between ZCS-QRCs and ZVS-QRCs [1], [11]. For example, the boost ZVS-QRC is the dual of the buck ZCS-QRC. A comparison of the waveforms shown in Figs. 8 and 11, clearly displays the duality relationship between them. In fact, the dual properties between them are not only true qualitatively, but also are true quantitatively. For example, the voltage-conversion ratio of the boost ZVS-QRC can be derived

from that of the buck ZCS-QRC simply by applying the duality principle.

The duality relationships also exist between any given converter in the ZCS-QRC family and its counterpart in the ZVS-QRC family.

Table I summarizes the major characteristics of the zero-current switching and zero-voltage switching techniques.

Table 1

	Zero-Current Switching	Zero-Voltage Switching
Control	constant on-time	constant off-time
Switch voltage waveform	quasi-square	quasi-sinusoidal
Switch current waveform	quasi-sinusoidal	quasi-square
Load range	[*R*min, *R*∞]	[0, *R*max]
V_0/V_i increases as	f_s increases	f_s decreases
V_0/V_i increases as	R_0 increases	R_0 increases
Full-wave mode	*D*1 in antiparallel with *Q*1	*D*1 in series with *Q*1
Half-wave mode	*D*1 in series with Q1	*D*1 in antiparallel with *Q*1

B. Experimental Results

1) ZCS-QRCs: A number of ZCS-QRCs have been built for various off-line power supplies as well as dc-dc converter applications [1], [3], [9], [10]. Due to the inherent capacitive turn-on loss, switching noise due to *dv/dt* (Miller effect) and reverse recovery of diodes in the circuit, the maximum operating frequency of ZCS-QRCs is limited to 1–2 MHz for off-line applications.

A half-bridge, 300-V, dc, off-line ZCS-QRC operating in both half-wave mode and full-wave mode was designed and fabricated in both broadboard and thick-film hybrid form [9], [10]. Using the leakage inductance of the transformer and secondary-side resonance, the circuit delivered 80 W (5 V/16 A) at 74 percent efficiency with a power density of 21 V/in. Other topologies, such as forward and flyback ZCS-QRCs, have also been breadboarded and results reported in [1] and [3]. A version of the forward ZCS-QRC operating in half-wave mode was reported earlier [8] and is available in various commercial and military off-line power supplies.

For ease of comparison, a flyback ZCS-QRC breadboard performance is presented here [1], so this circuit can be directly compared with a flyback ZVS-QRC in the following section.

A flyback converter topology which utilizes the leakage inductance of the step-down transformer as the resonant element L_r is shown in Fig. 14(a). In addition, resonance capacitor C_r is placed across the secondary winding.

A 1.0-MHz 75-W flyback resonant converter was implemented. The circuit diagram with the parts list is shown in Fig. 14(a). Resonant frequency is chosen at 2.86 MHz and characteristic impedance at 35 Ω. With an input voltage of 150 V and a load resistance of 2.0 Ω, the output voltage reaches 12.0 V when the switching frequency is 1.0 MHz.

Waveforms in Fig. 14(b) show that the peak drain-to-source voltage is 330 V and the peak input current is about 4 A. Oscillations in the current and secondary voltage waveforms are believed to be caused by resonance between the transformer leakage inductance and various parasitic

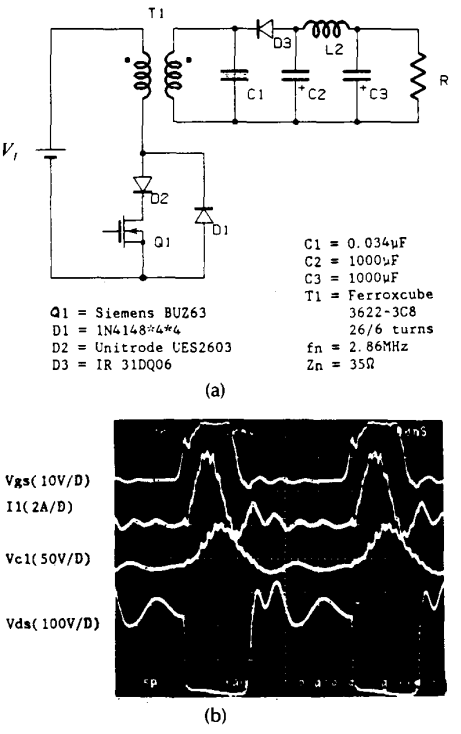

Fig. 14. (a) Implementation of a 1.0-MHz 75-W flyback resonant converter with *T*1 leakage inductance providing resonant inductance. (b) Waveforms of the new ZVS-QRCs flyback resonant converter.

capacitances including the winding stray capacitance and junction capacitances (of the semiconductor devices).

Efficiency of the power stage at full load is measured at 84 percent. Estimation of power losses are: 5 W for output rectifier D_3, 2 W for transformer T_1, 5.5 W for switch Q_1, and 1.5 W for stray losses.

2) ZVS-QRCs: The ZVS technique produces high voltage stress across the power switch(es). Therefore, single-ended topologies are not suitable for off-line applications. However, due to the reduced switching stresses, losses, and switching noises, the ZVS-QRCs are capable of operating at a higher frequency. The single-ended ZVS-QRCs are particularly suited for high-density high-performance dc-dc conversion for telecommunication, automotive, and on-board power supply applications. Certain ZVS-QRCs can be extended for off-line applications. These configurations usually employ more than one power switch. For example, a half-bridge ZVS-QRC has been built for this purpose [13]. The peak stress across the power switches is limited to the supply voltage in this configuration because the conduction of one switch automatically clamped the voltage across the off-switch at the magnitude of the supply voltage.

For the purpose of comparison with the flyback ZCS-QRC presented earlier, performance of a flyback ZVS-QRC breadboard is demonstrated here. A flyback ZVS-QRC was breadboarded with the following specifications:

- output voltage V_0 = 5 V,
- input voltage range V_{IN} = 40–60 V,
- load resistance range R_L = 1.25–5 Ω,
- maximum switching frequency f_{smax} = 13 MHz.

The circuit diagram of the converter including gate drive and VCO is shown in Fig. 15.

There are no external resonant components in the circuit. The resonant inductance is formed entirely by the intrinsic

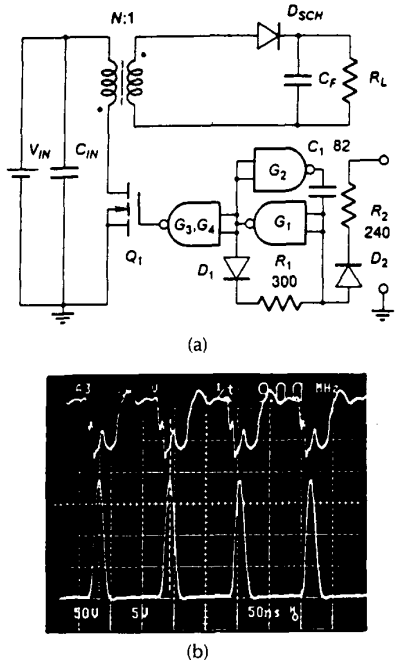

Fig. 15. (a) Circuit diagram of the flyback ZVS-QRC. (b) Gate-to-source voltage (top, 5 V/div) and drain-to-source voltage (bottom, 50 V/div) waveforms at P_{OUT} = 10 W, V_{IN} = 5 V. Time scale: 50 ns/div. Q_1 = IRF720 (International Rectifier); C_{iss} = 600 pF at V_{GS} = 5 V; C_{oss} = 32 pF at V_{DS} = 40 V. D_{SCR} = 2 × IR31DQ06 (International Recitifer). C_{IN} = 0.1-μF stack metal film capacitor. C_F = 3.3-μF multilayer ceramic (Z5U) chip capacitor. T_r = 6:1 turns on P14/8-A 160-H6F (primary—AWG 22, secondary—copper ribbon 5 mils thick, 160 mils wide).

inductances of the circuit: the leakage inductance of the transformer and the lead inductances of D_{SCH}, $C_{in}C_F$, and the MOSFET. The total value of L_r (as seen at the primary side of the transformer) was estimated as 2.5 μH. The resonant capacitor is formed by the transistor's output capacitance and the winding capacitance of the transformer. The total value of C_r was estimated as 40 pF. The characteristic impedance and resonant frequency are 250 Ω and 16 MHz, respectively. The slow-recovery body diode of the MOSFET can be used in the circuit to form a bidirectional switch. This is possible since immediately after the body diode is turned off the MOSFET transistor is turned on, which shorts the body diode permitting the minority carriers to recombine internally.

The circuit is operated in an open-loop fashion; a 5-V output is obtained by varying the switching frequency. When the output power is less than 5 W, even through the output voltage still can be regulated, the ZVS property can no longer be achieved. Efficiency of the power stage is around 70 percent for medium and high loads. Efficiency will drop below 60 percent at light loads when the ZVS property is lost.

Typical experimental waveforms of gate-to-source voltage and drain-to-source voltage are shown in Fig. 15(b). Notice that the waveforms are extremely clean (free of switching noise) at 9 MHz. No Miller effect or switching induced *dv/dt* or *di/dt* is observed in this breadboard. Consequently, the circuit is capable of operating at a switching frequency much higher than that of the ZCS-QRCs.

VI. Gate-Drive Design

A gate drive is an important part of any high-frequency converter design. There are several problems associated with high-frequency gate drives [12].

1) Switching devices in the gate drive. To reduce the dynamic losses in a power MOSFET, turn-on and/or turn-off times should be minimized. For a given MOSFET this can be achieved only by increasing the charging/discharging gate current during turn-on/off. Increased charging/discharging gate current requires larger (i.e., slower) gate-drive devices. Since the switching devices in the gate-drive circuit should be substantially faster and easier to drive than the power MOSFET, there are practical limitations of the maximum gate current achieved during turn-on/off.

2) Parasitic inductances. To achieve rapid change of the gate current during turn-on/off, the inductance in the gate-current loop should be as low as possible. Therefore, the devices used in the gate-drive, as well as the power MOSFET, should have minimum lead inductances. Packaging of the devices and layout of the circuit are important factors affecting the switching speed. Surface mount and thick-film hybrid technologies can help to reduce parasitic inductances.

3) Power dissipation in the gate-drive circuit. Turning a MOSFET on/off requires charging/discharging the MOSFET's input capacitance C_{iss}. In general, C_{iss} is nonlinear. Although in the following discussion C_{iss} is assumed to be constant, the conclusions are identical for a nonlinear C_{iss}. In most high-speed gate-drive circuits, the charging/discharging of C_{iss} is achieved by connecting the gate through lower impedance switches to positive and negative potentials, V_{ON} and V_{OFF}, respectively. Every time the MOSFET is turned on/off the energy

$$E_G = \tfrac{1}{2}(V_{ON}^2 + V_{OFF}^2)C_{iss} \tag{9}$$

is dissipated in the gate-drive circuit. Power dissipation in the gate-drive circuit is proportional to the switching frequency

$$P_G = 2f_S E_G. \tag{10}$$

Switching speed can be increased by increasing the differential voltage, $V_{ON} - V_{OFF}$. However, this would substantially increase power dissipation in the gate-drive circuit. Therefore, V_{ON} should be only as high as necessary to saturate the MOSFET and V_{OFF} should be sufficiently low to cut it off. From (10) it can be seen that an increased switching frequency results in an increased power dissipation in the gate drive. Thus, gate-drive devices should have appropriate power ratings and often need heat sinks. A higher power rating of a device usually implies lower switching speed, while the presence of heat sinks usually contributes to an increase in wiring inductance in the gate-drive circuit. Therefore, reduction of power dissipation in the gate-drive circuit is essential to increase its speed.

Power dissipation in the gate-drive circuit can be reduced by charging and/or discharging C_{iss} using a resonant tech-

nique. In some cases, a resonant approach can improve switching characteristics of the gate drive [21]. Theoretically, an inductance introduced in series with the gate and appropriately resonant with C_{iss} could reduce power dissipation in the gate drive [22]. Unfortunately, as mentioned, any inductance in series with the gate inevitably reduces switching speed.

A novel, quasi-resonant, gate-drive circuit suitable for high-frequency quasi-resonant converters is proposed. It is observed in QRCs that fast switching is critical either during turn-on or during turn-off, but not during both. For example, in the ZVS-QRCs operating in half-wave mode, the turn-off time is critical because the switching loss, caused by the nonzero product of the drain-to-source voltage and the drain current, occurs only during turn-off. In ZCS-QRCs, turn-on speed is more critical. Therefore, in ZVS-QRCs, the fall time of the gate-to-source voltage should be minimized to achieve fast turn-off. Rise time of the gate-to-source voltage, however, is not as critical since turn-on occurs during the conduction period of diode D_S which occupies a substantial portion of the switching period. Thus fast turn-off can be achieved in a conventional, dissipative manner, while turn-on can be obtained using a resonant technique. Such operation of the gate drive should theoretically reduce power dissipation in the gate-drive circuit by half.

A circuit implementation of the quasi-resonant gate drive is shown in Fig. 16. The gate-drive circuit consists of a single

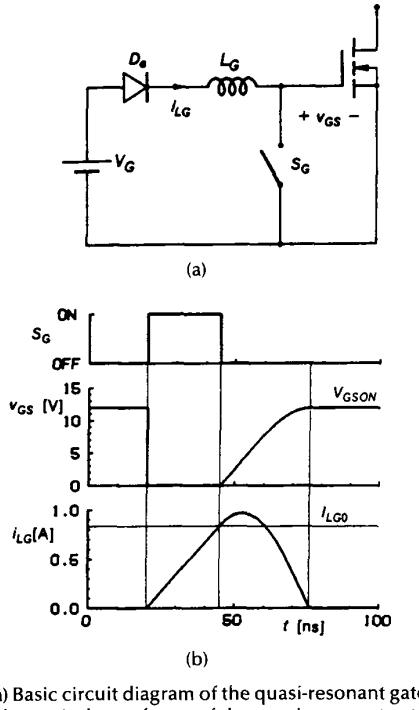

Fig. 16. (a) Basic circuit diagram of the quasi-resonant gate drive. (b) Theoretical waveforms of the quasi-resonant gate drive at V_G = 4 V, L_G = 120 nH, and C_{iss} = 1.8 nF.

supply voltage, one switch, a diode, and a resonant inductor. The operation of the circuit is as follows. When switch S_G is on, the MOSFET is off and voltage V_G is applied to inductance L_G. During this stage, which lasts as long as the fixed off-time of the MOSFET, current in the inductance builds up and eventually reaches I_{LGO}, as shown in Fig. 16(b). When S_G turns off, L_G and C_{iss} form a resonant circuit and V_{GS} increases in a resonant fashion. When current i_{LG} reaches zero, resonance is stopped by diode D_G. Since turn-on is achieved through the resonance of L_G and C_{iss}, the power dissipation in the gate drive is reduced approximately by half compared to conventional gate-drive circuits. The dual network of Fig. 16(a) would be suitable for ZVS-QRCs.

VII. Closed-Loop Control

A. Single-Loop-Controlled QRC

Closed-loop regulation of the output voltage of the QRC can be achieved by feedback of the output voltage. The small-signal performance of the QRC power stage can be analyzed by the method given in [20].

A commonly-used, single-loop control scheme for the buck QRC power stage described earlier is shown in Fig. 17.

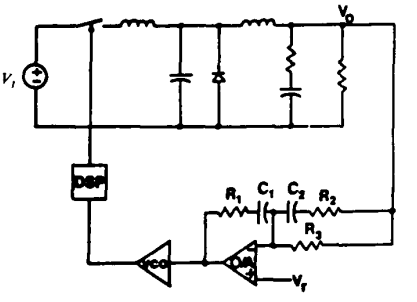

Fig. 17. Single-loop-controlled QRC with voltage-controlled oscillator.

A two-pole two-zero compensation network is used for this circuit to provide high low-frequency gain and improved phase margin at the cross-over frequency. The output filter capacitor suitable for high-frequency QRCs usually has a very low equivalent series resistance (ESR). The zero due to this ERS usually occurs above the switching frequency and does not improve the phase margin.

The output of the error amplifier controls the VCO to determine the frequency of operation. The control block, DSP (Digital Signal Processor), consists of switch drive circuitry and logic which converts the output signal of the VCO into a constant on-time pulse for ZCS and a constant off-time pulse for ZVS.

This single-loop control has several disadvantages:

- The VCO requires a considerable number of components. The effective bandwidth of the control is limited by noise considerations: a VCO can be sensitive at higher frequencies and a large amount of ripple is transmitted through a high-gain amplifier.
- The undamped buck QRC and the boost and buck-boost QRCs can be very difficult to compensate. Bandwidth and good closed-loop performance must be traded off against stability. Boost and buck-boost converters are especially difficult to control since they have a right-half-plane zero in the control-to-output transfer function. This zero places severe limitations on the bandwidth of the control loop and, therefore, good closed-loop performance is difficult to achieve.

B. Multi-Loop-Controlled QRC [23]

Multi-loop control (or current-mode control) offers significant improvement in closed-loop response for PWM converters [24]. A similar scheme is described in this paper for the control of QRCs. Referred to as *current-sensed frequency control* (CSFC), this control, as shown in Fig. 18,

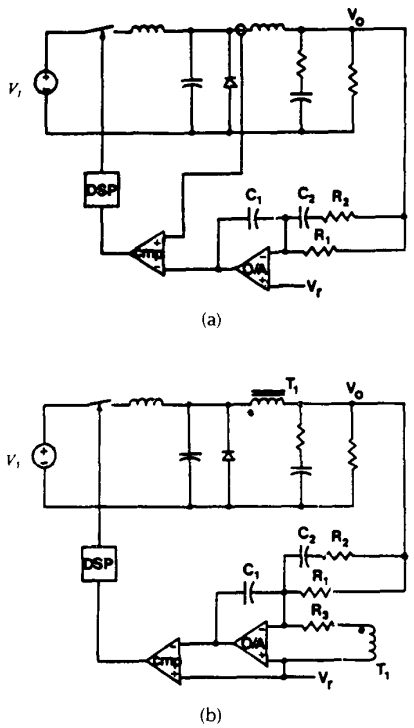

Fig. 18. Multi-loop current-sensed frequency control scheme for QRCs. (a) Direct inductor sensing. (b) AC current sensing.

compares a signal proportional to the output-filter inductor current with an error voltage signal to modulate the switching frequency. CSFC offers the same advantages as current-mode control for PWM converters with the additional benefits of eliminating the VCO and increased noise immunity.

The continuous filter-inductor current is sensed directly. For example, if this control is implemented in ZCS-QRCs, when the down-slope of this current intersects the control error voltage, the power switch is turned on. Using this multi-loop control, the circuit can be stabilized with a single-zero, two-pole compensation network. The VCO is replaced with a simple comparator whose operation is far less noise sensitive.

Like current-mode control for PWM converters [24], several possible ways of implementing CSFC exist. The most direct method uses resistive sensing with an operational amplifier, but this can be expensive, inefficient, and quite impractical for higher power outputs.

A second method uses a current transformer in series with diode D_1. A current transformer can be used since the diode current is discontinuous and equal to the filter inductor current during the free wheeling stage. This control implementation can be used for current sharing and current limiting, but it may be difficult to implement, due to these high-amplitude step waveforms which generate considerable noise. This problem is commonly experienced with PWM converters with current-transformer sensing and will be worse for high-frequency operation of QRCs.

If current limiting and current sharing are not required, the most simple and effective implementation of CSFC can be achieved as shown in Fig. 18(b). Here, the inductor *voltage* is sensed and integrated through R_3, and C_1 to reconstruct the inverted ac portion of the inductor current. This is summed through the operational amplifier with the error voltage and compared to a fixed reference. This implementation of CSFC is analogous to the Standard Control Module (SCM) for constant on-time PWM converters [24]. The circuit is inherently noise-free due to the integration of all control voltages and will probably be the most useful for zero-voltage-switched converters operating at frequencies around 10 MHz.

Ignoring second-order effects, all three implementations of CSFC offer *identical* small-signal characteristics for the circuit. The particular implementation of CSFC does not, therefore, affect the transient response of the circuit.

VIII. Conclusions

As the switching frequency is boosted into the megahertz range, the abrupt switching approach used in the conventional PWM converter encounters formidable difficulties. In particular, the switching stresses and losses, which are suppressed by means of scrubber circuits or ignored at lower frequencies, become intolerable at high-frequency operations.

To alleviate switching stresses and losses, the concept of the resonant switch was introduced and implemented either in the form of zero-current switching (ZCS) or zero-voltage switching (ZVS). By direct application of the resonant switch(es) into PWM converters, a new family of quasi-resonant converters (QRCs) have been discovered. This new family of converters with literally hundreds of topological variations can be viewed as hybrids of PWM and conventional resonant converters. They utilize the principle of inductive or capacitive energy storage and transfer for power conversion in a fashion similar to PWM converters. However, an *LC* tank circuit is always present in conjunction with the power switch and is used not only to shape the current and voltage waveforms but, also, to store and transfer energy from input to output in a manner similar to the conventional resonant converters. For this reason, the QRCs are regulated only with the use of a frequency modulation (FM) technique.

This family of QRCs can be divided into two classes, one class is referred to as ZCS-QRCs employing ZCS concept; the other referred to as ZVS-QRCs employ the ZVS concept. ZCS-QRCs and ZVS-QRCs again can be subdivided into two categories: full-wave (FW) mode and half-wave (HW) mode, depending upon whether the power switch is unidirectional or bidirectional. It has been shown that the FW-QRCs are load insensitive. Therefore, the switching frequency is maintained constant as the load varies. However, the HW-

QRCs, are load sensitive. As the load varies, the switching frequency has to be modulated over a wide range to maintain output-voltage regulation.

For off-line applications and for switching frequencies up to 1 MHz, the ZCS technique is very effective since it eliminates the switching stresses and turn-off losses. Employing the ZCS technique, a 1-MHz 100-W off-line converter was developed which achieved a power density of 25 W/in^3. This technique results in a switch current waveform which is quasi-sinusoidal and a switch voltage waveform which is quasi-square wave. The device's voltage stress is minimum but its conduction loss is higher than that of PWM converters. To operate the semiconductor switches at a higher frequency, the capacitive turn-on loss associated with ZCS must be avoided.

To minimize the capacitive turn-on loss, the ZVS technique was proposed. This technique allows the power switches to turn-on under zero-voltage condition and, therefore, eliminate the turn-on loss associated with the parasitic junction capacitances. Since the power switch is always turned on at zero-voltage, a simple capacitor snubber (in many cases, C_{ds} of the MOSFET) can be used to minimize turn-off loss and, thus, achieve a zero-voltage turn-off condition. The ZVS technique offers several distinct advantages:

- Elimination of switching losses and stresses while achieving high efficiency by keeping the device's conduction loss minimal.
- Elimination of *dv/dt* and *di/dt* noises due to device switching. The *dv/dt* noise is often coupled into the drive circuit by means of the Miller effect and is one of the primary limiting factors for designing at very high frequencies.
- Reduction of EMI.

It is important to note that all the merits can be achieved by utilizing the parasitic elements in the circuits such as the transformer's leakage inductance and semiconductor junction capacitances. Furthermore, the slow-recovery body diode of the MOSFET can be used in the circuit due to the nature of zero-voltage switching. Consequently, the converter circuits are remarkably simple. Since the ZVS technique results in a quasi-square current waveform and quasi-sinusoidal voltage waveform, the conduction loss is minimized but the peak voltage stress across the switch can be several times higher than that of the PWM converter. Consequently, the single-ended converter topologies are not suited for off-line applications. The technique is particularly suited for distributed, on-board, dc-dc converters where high power density is most desired. Practical ZVS-QRCs have been implemented operating in frequencies over 10 MHz.

Other important design aspects of high-frequency QRCs have been addressed. A new quasi-resonant gate-drive for MOSFETs is proposed. This simple drive scheme enables fast switching while reducing the power consumption in the gate circuit by half compared to conventional gate drives. A new, multi-loop control, analogous to current mode control for PWM converters, has also been developed for QRCs. The new control provides a rugged system with excellent transient response and noise immunity. The need for a VCO, which can be difficult to implement at high frequencies, is eliminated.

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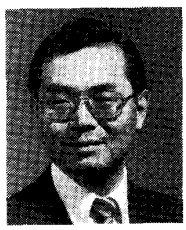

Fred C. Lee (Senior Member, IEEE) received the B.S. degree in electrical engineering from Chen-Kung University, Taiwan, Republic of China, in 1968. He received the M.S. and Ph.D. degrees in electrical engineering from Duke University, Durham, NC, in 1971 and 1974, respectively.

From 1974 to 1977, he was employed as a member of the Technical Staff of Control and Power Processing Department, TRW Systems, where he was engaged in design, simulation, and analysis for spacecraft power processing equipment. In 1977, he joined Virginia Polytechnic Institute and State University. He is presently the James S. Tucker Endowment Professor and the Director of the Virginia Power Electronics Center. His research interests include power electronics, power semiconductor devices, electric vehicle propulsion, resonant power processors for high-power and high-frequency applications, nonlinear modeling, analysis, and design optimization for power processing equipment and systems. He has published over 100 articles in the areas of power device and circuit modeling, analysis, and design.

Dr. Lee is Vice President of the IEEE Power Electronics Society, an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, and a member of the IEEE AES Power/Energy Panel. He was the Chairman of the 1987 IEEE International Power Electronics Conference. He is the recipient of the Society of Automotive Engineering 1985 Ralph R. Teeter Educational Award.