Design Guide: TIDA-010054

Bidirectional, Dual Active Bridge Reference Design for Level 3 Electric Vehicle Charging Stations

TEXAS INSTRUMENTS

Description

This reference design provides an overview on the implementation of a single-phase Dual Active Bridge (DAB) DC/DC converter. DAB topology offers advantages like soft-switching commutations, a decreased number of devices and high efficiency. The design is beneficial where power density, cost, weight, galvanic isolation, high-voltage conversion ratio, and reliability are critical factors, making it ideal for EV charging stations and energy storage applications. Modularity and symmetrical structure in the DAB allow for stacking converters to achieve high power throughput and facilitate a bidirectional mode of operation to support battery charging and discharging applications.

Resources

TIDA-010054	Design Folder
UCC21530, AMC1311, AMC3302	Product Folder
AMC3306M05, LM76003, SN6505B	Product Folder
ISO7721, LMZ31707, TPS7B69	Product Folder
OPA320, REF2033, SN6501	Product Folder
TL431, SN74LVC2G34, TMS320F280049	Product Folder

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Features

- Single-phase-shift, DAB
- Dual-channel UCC21530 with reinforced isolation used for driving SiC MOSFETs in the half-bridge configuration
- TMS320F280049 controller for implementation of digital control
- Isolated voltage and current sensing
- Maximum power output of 10 kW
- Full load efficiency of 97.6% and a peak efficiency of 98.2% at 6 kW
- High-power density of 2.32 kW/L
- Primary voltage of 700-800-V DC, secondary voltage of 380-500-V DC
- Two-level turnoff for short-circuit protection with adjustable current limit and delay (blanking) time
- PWM switching frequency of 100 kHz and reduced transformer size enabled by planar magnetics
- Soft switching without auxiliary components

Applications

- DC charging (pile) station
- EV charging station power module
- Energy storage power conversion system (PCS)
- On-board (OBC) and wireless charger
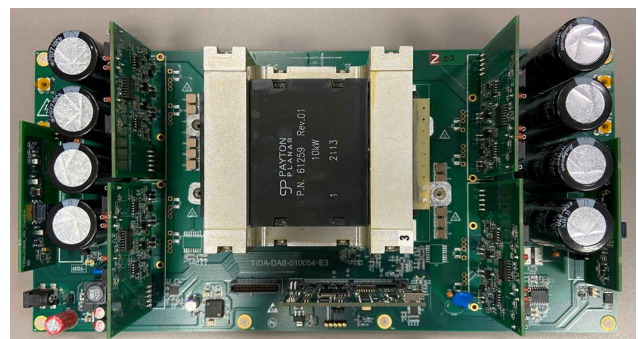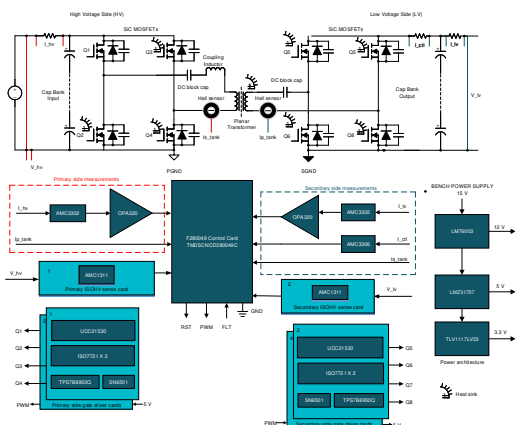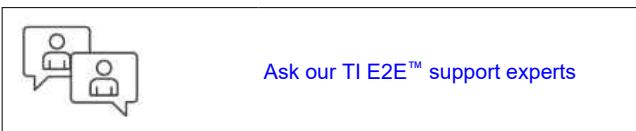
1 System Description

The electric vehicle charging standards governed by the Combined Charging System and CHAdeMO® are constantly changing and are pushing for faster battery charging rates requiring typically less than 30 minutes spent at a charging station for one full charge of an electric vehicle. The DC charging station is typically a Level 3 charger which can cater to a very high power level between 120–240 kW. These DC charging stations are standalone units which house AC/DC and DC/DC power conversion stages. A number of power conversion modules are stacked together inside of a charging station to increase the power levels and enable fast charging. DC fast-charging stations provide a high power DC current to an electric vehicle's battery without passing through any onboard AC/DC converter, which means the current is connected directly to the battery. Most cars on the road today can handle only up to 50 kW. Newer cars will have the ability to charge at greater rates of power. As EVs come with higher range and batteries get bigger, DC charging solutions are being developed to support long-range EV batteries through fast charging stations up to 120 kW or more.

The DC/DC converter in a charging station must be capable of interfacing with the rectified bus voltage (700-800 V) from a three-phase Vienna rectifier at its input and connect with the battery of an electric vehicle at its output, delivering rated power. The DC/DC converter finds important application in a number of end equipment. Figure 1-1 shows its use in charging stations, solar photovoltaic systems, energy storage systems, and electric vehicle traction applications.
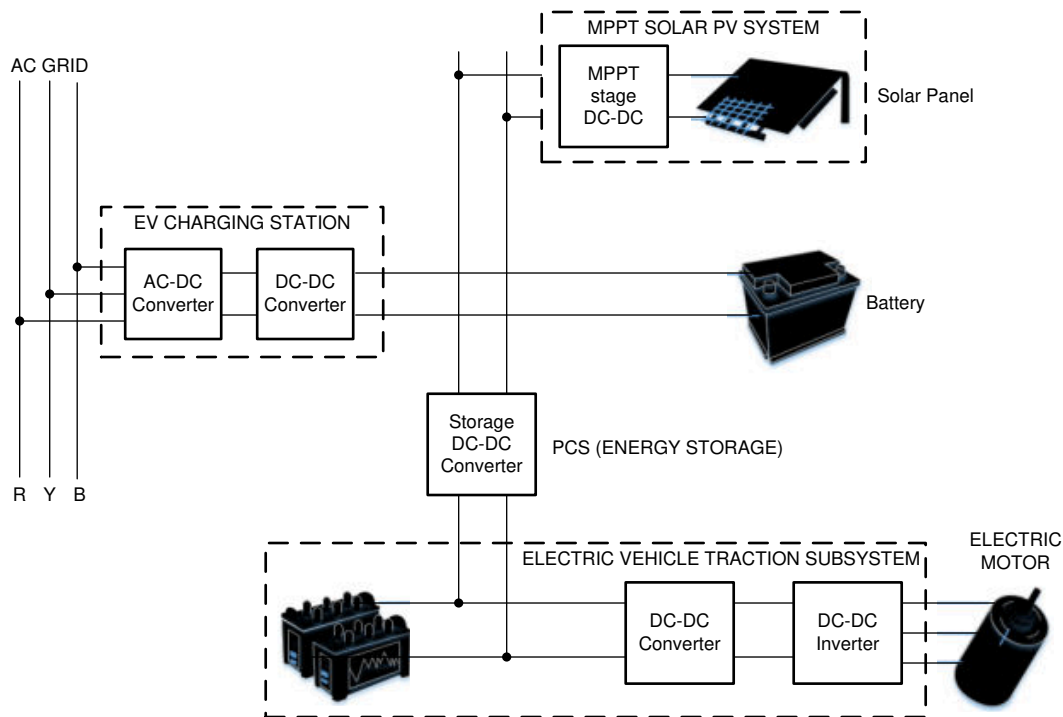

Figure 1-1. Role of DC/DC Converter

The DC/DC converter must be capable of handling high power levels. In addition to this, the converter must be modular, which enables single power stage converter units to be paralleled, whereby the output power throughput can be scaled to higher levels as required by DC charging station standards. Current trends in the charging station are moving toward converters that can handle bidirectional power flow. New practices, such as Vehicle-to-Grid (V2G), involve power transfer between the battery of an electric vehicle and the AC grid. Bidirectional DC/DC converters enable charging of the battery in the forward mode of operation and facilitate flow of power back to the grid from the battery during reverse mode of operation, which can be used to stabilize the grid during peak load periods.

Power density and system efficiency are two important requirements of a converter in a DC charging station. Operating at high switching frequencies enables reduced size of magnetics. By moving to higher bus voltage to facilitate fast charging, more power can be transferred at the same current level. This helps to reduce the amount of copper, thereby improving power density of the converter. The converter must also be highly efficient

as it results in significant cost savings and reduced thermal solution. This reduced thermal solution directly translates into reduced and compact heat sink size, which in turn increases the power density of the converter. The converter must also be capable of inherent soft switching like ZVS (Zero Voltage Switching) and ZCS (Zero Current Switching) without the addition any bulky passive components which might hamper power density.

The DC/DC converter must be capable of interfacing seamlessly with Lithium ion or a lead acid battery, which are predominantly used in EV charging stations. The DC/DC converter must also be capable of providing the required voltage conversion between the high-voltage and low-voltage side and provide galvanic isolation between them.

Traditional switching devices have a limit on how quickly they can switch high voltages, or more appropriately, the dV/dt ability of the device. This slow ramping process increases switching loss because the device spends more time in switching transition. This increased switch time also increases the amount of dead time required in the control system to prevent shoot-through and shorts. The solution to this has been developed in newer switching semiconductor technology such as SiC and GaN devices with high electron mobility. This reference design uses SiC MOSFETs alongside TI's SiC gate driver technology to demonstrate the potential benefits it translates when it comes to efficiency and power density.

The following four popular topologies were considered for analysis.

- LLC resonant converter
- Phase-shifted, full bridge
- Single-phase, dual-active bridge
- Dual-active bridge in CLLC mode

Based on this study, the dual-active bridge was chosen for implementation in this reference design, owing to its ease of bidirectional operation, modular structure, competitive efficiency, and power density numbers with respect to other competing topologies. This reference design focuses on addressing the challenges when designing a high-power, dual-active-bridge DC/DC converter for the EV charging station.

1.1 Key System Specifications

Table 1-1 lists some of the critical design specifications of the dual-active-bridge (DAB) DC/DC converter. The system has a full load efficiency of 97.6% at an output power of 10 kW.

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	700-800-V DC	Section 3.1
Output voltage range	380-500-V DC	Section 3.1
Output power rating	10-kW maximum	Section 2.3.5
Output current	26-A maximum	Section 2.3.5
Efficiency	Peak 98.2% (at 6.6 kW) full load 97.6% (at 10 kW)	Section 4.5
PWM switching frequency	100 kHz	Section 2.3.4.6
Power density	>2 kW/L	Section 4.5
Voltage ripple	<5 %	Section 2.3.4.4

Table 1-1 shows that the input voltage range is between 700 V and 800 V. This range was considered because the DC/DC converter must interface with the front-end Vienna rectifier and the three-phase power factor correction (PFC), which has an output that is within this range. This converter can also be used in conjunction with single-phase PFC systems with an output that is in the range of 400 V, which must interface with 48- and 72-V batteries.

2 System Overview

This section shows the block diagram of the dual-active-bridge DC/DC converter.
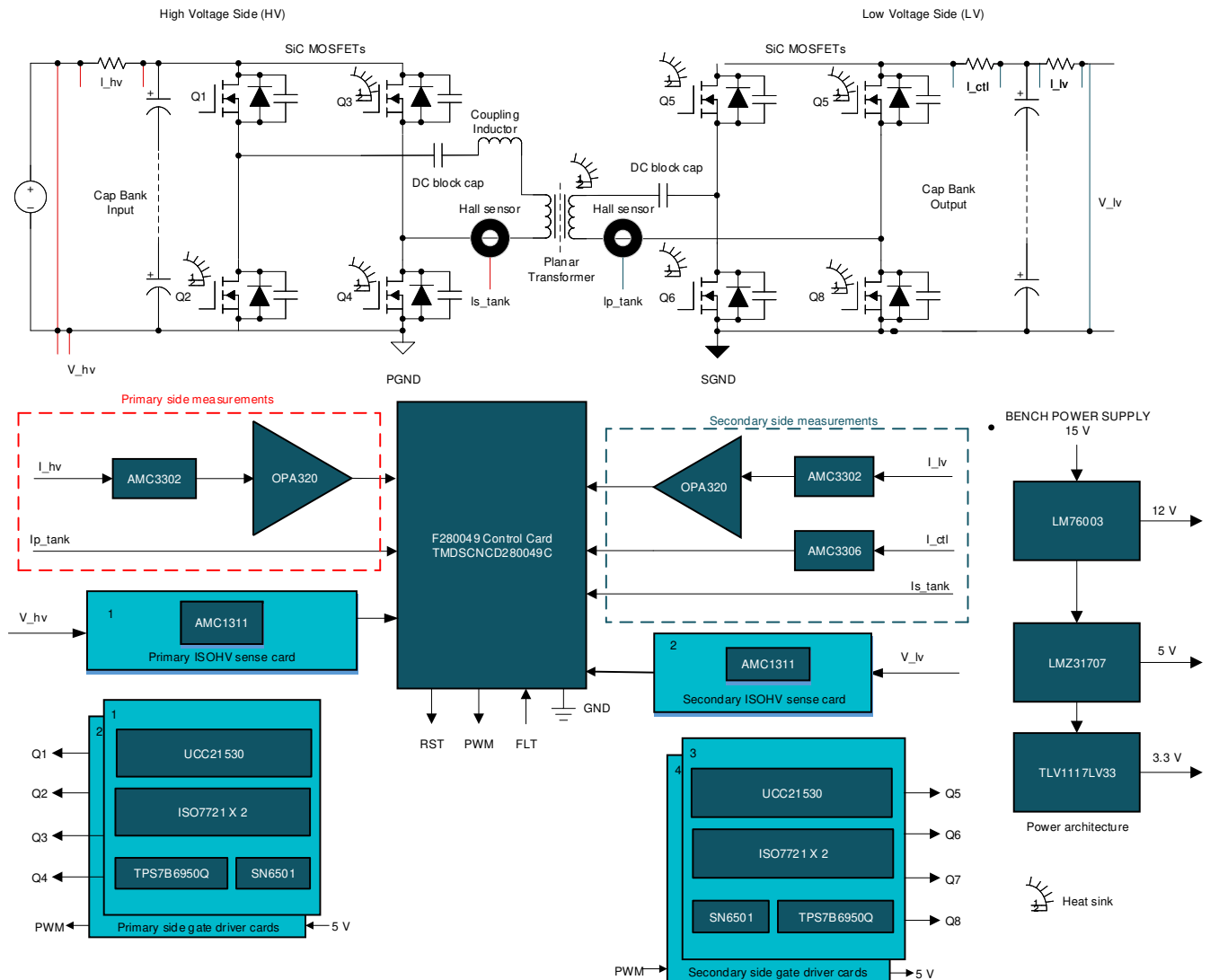
2.1 Block Diagram

Figure 2-1. TIDA-010054 Block Diagram

This reference design consists of four main sections that intercommunicate:

- A power board comprising the power stage SiC MOSFETs, a high frequency transformer, current sensing electronics, and the system power tree
- A TMDSCNCD280049C control card to support digital control
- Four gate driver cards, each having a UCC21530 to drive the four legs of the DC/DC converter
- Two isolated high-voltage (ISOHV) sensing cards, each having an AMC1311 device to sense the input/output bus voltage

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Note

The isolated high-voltage (ISOHV) sensing card is a reuse of the design from TIDA-01606 Rev. E4 ISOHV card.

2.2 Highlighted Products

This section highlights the critical components of the design which include the gate driver, F280049 controller, isolated amplifiers for current and voltage sensing, and generating voltage references.

2.2.1 UCC21530

The UCC21530 is used for driving the SiC MOSFETs of the power stage. The device is an isolated dual-channel gate driver with 4-A source and 6-A sink peak current. The UCC21530 is designed to drive IGBTs and SiC MOSFETs up to 5 MHz with best-in-class propagation delay of 19 ns and pulse-width distortion of 5 ns. The input side is isolated from the two output drivers by a 5.7-kV$_{RMS}$ reinforced isolation barrier, with a minimum of 100-V/ns common-mode transient immunity (CMTI). Internal functional isolation between the two secondary-side drivers allows a working voltage of up to 1850 V. The device accepts VDD supply voltages up to 25 V. A wide input VCCI range from 3 V to 18 V makes the driver suitable for interfacing with both analog and digital controllers.

For more details on this device, see the UCC21530 product page.

2.2.2 AMC1311

The AMC1311 is used for DC voltage sensing at the input and output terminals. The device is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7-kV peak according to VDE V 0884-1 and UL1577. The high-impedance input of the AMC1311 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance. The excellent performance of the device supports accurate, low temperature drift voltage or temperature sensing and control in closed-loop systems.

For more details on this device, see the AMC1311 product page.

2.2.3 AMC3302

The AMC3302 is a precision, isolated amplifier optimized for shunt-based current measurements. The fully integrated, isolated DC/DC converter allows single-supply operation from the low-side of the device, which makes the device a unique solution for space-constrained applications. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577 and supports a working voltage of up to 1.2 kV$_{RMS}$. The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage. The input of the AMC3302 is optimized for direct connection to a low-impedance shunt resistor or another low-impedance voltage source with low signal levels. The excellent DC accuracy and low temperature drift supports accurate current measurements over the extended industrial temperature range from –40°C to +125°C. The integrated DC/DC converter fault-detection and diagnostic output pin of the AMC3302 simplify system-level design and diagnostics.

For more details on this device, see the AMC3302 product page.

2.2.4 AMC3306M05

The AMC3306M05 is a precision, isolated delta-sigma (ΔΣ) modulator, optimized for shunt-based current measurements. The fully integrated, isolated DC/DC converter allows single-supply operation from the low-side of the device, which makes the device a unique solution for space-constrained applications. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577 and supports a working voltage of up to 1.2 kV$_{RMS}$. The isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects the low-voltage side from hazardous voltages and damage. The input of the AMC3306M05 is optimized for direct connection to a low-impedance shunt resistor or other, low-impedance voltage sources with low signal levels. The excellent DC accuracy and low temperature drift support accurate current measurements over the extended industrial temperature range from –40°C to +125°C. By using a digital filter (such as those in the TMS320F2807x orTMS320F2837x microcontroller families) to decimate the bitstream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB at a data rate of 78 kSPS.

For more details on this device, refer the AMC3306M05 product page.

2.2.5 LM76003

The LM76002, LM76003 regulator is an easy-to-use synchronous step-down DC/DC converter capable of driving up to 2.5 A (LM76002) or 3.5 A (LM76003) of load current from an input up to 60 V. The LM76002, LM76003 provides exceptional efficiency and output accuracy in a very small solution size. Peak current-mode control is employed. Additional features such as adjustable switching frequency, synchronization, FPWM option, power-good flag, precision enable, adjustable soft start, and tracking provide both flexible and easy-to-use solutions for a wide range of applications. Automatic frequency foldback at light load and optional external bias improve efficiency. This device requires few external components and has a pinout designed for simple PCB layout with best-in-class EMI (CISPR22) and thermal performance. Protection features include input undervoltage lockout, thermal shutdown, cycle-by-cycle current limit, and short-circuit protection. The LM76002, LM76003 device is available in the WQFN 30-pin leadless package with wettable flanks.

For more details on this device, refer the LM76003 product page.

2.2.6 LMZ31707

The LMZ31707 SIMPLE SWITCHER® power module is an easy-to-use integrated power solution that combines a 7-A DC/DC converter with power MOSFETs, a shielded inductor, and passives into a low profile, QFN package. This total power solution allows as few as three external components and eliminates the loop compensation and magnetics part selection process. The 10-mm × 10-mm × 4.3-mm QFN package is easy to solder onto a printed circuit board and allows a compact point-of-load design. Achieves greater than 95% efficiency and excellent power dissipation capability with a thermal impedance of 13.3°C/W. The LMZ31707 offers the flexibility and the feature-set of a discrete point-of-load design and is ideal for powering a wide range of ICs and systems. Advanced packaging technology affords a robust and reliable power solution compatible with standard QFN mounting and testing techniques.

For more details on this device, refer the LMZ31707 product page.

2.2.7 OPA320

The OPA320 (single) and OPA2320 (dual) are a new generation of precision, low-voltage CMOS operational amplifiers optimized for very low noise and wide bandwidth while operating on a low quiescent current of only 1.45 mA. The OPA320 series is ideal for low-power, single- supply applications. Low-noise (7 nV/√Hz) and high-speed operation also make them well-suited for driving sampling analog-to-digital converters (ADCs). Other applications include signal conditioning and sensor amplification. The OPA320 features a linear input stage with zero- crossover distortion that delivers excellent common- mode rejection ratio (CMRR) of typically 114 dB over the full input range.

For more details on this device, refer the OPA320 product page.

2.2.8 ISO7721

The ISO772x devices are high-performance, dual-channel digital isolators with 5000 V_{RMS} (DW and DWV packages) and 3000 V_{RMS}(D package) isolation ratings per UL 1577. The ISO772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO2) insulation barrier. They support up to 100 Mbps data rate and have low propagation delay 11-ns.

For more details on this device, refer the ISO7721 product page.

2.2.9 SN6501

The SN6501 is a monolithic oscillator/power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio. The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

For more details on this device, refer the SN6501 product page.

2.2.10 SN6505B

The SN6505x is a low-noise, low-EMI push-pull transformer driver, specifically designed for small form factor, isolated power supplies. The device drives low-profile, center-tapped transformers from a 2.25-V to 5-V DC power supply. Ultra-low noise and EMI are achieved by slew rate control of the output switch voltage and through Spread Spectrum Clocking (SSC). The SN6505x consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive ground-referenced N-channel power switches. The device includes two 1-A Power-MOSFET switches to ensure start-up under heavy loads. The switching clock can also be provided externally for accurate placement of switcher harmonics, or when operating with multiple transformer drivers. The internal protection features include a 1.7-A current limiting, under-voltage lockout, thermal shutdown, and break-before-make circuitry. SN6505x includes a soft-start feature that prevents high inrush current during power up with large load capacitors.

For more details on this device, refer the SN6505B product page.

2.2.11 TMP235

The TMP23x devices are a family of precision CMOS integrated-circuit linear analog temperature sensors with an output voltage proportional to temperature engineers can use in multiple analog temperature-sensing applications. These temperature sensors are more accurate than similar pin-compatible devices on the market, featuring typical accuracy from 0°C to +70°C of ±0.5°C and ±1°C. The increased accuracy of the series is designed for many analog temperature-sensing applications. The TMP235 device provides a positive slope output of 10 mV/°C over the full –40°C to +150°C temperature range and a supply range from 2.3 V to 5.5 V. The 9-µA typical quiescent current and 800-µs typical power-on time enable effective power-cycling architectures to minimize power consumption for battery-powered devices.

For more details on this device, refer the TMP235 product page.

2.2.12 LMT87

The LMT87 device is a precision CMOS temperature sensor with ±0.4°C typical accuracy (±2.7°C maximum) and a linear analog output voltage that is inversely proportional to temperature. The 2.7-V supply voltage operation, 5.4-µA quiescent current, and 0.7-ms power-on time enable effective power-cycling architectures to minimize power consumption for battery-powered applications such as drones and sensor nodes. The LMT87LPG through-hole TO-92S package fast thermal time constant supports off-board time-temperature sensitive applications such as smoke and heat detectors. The accuracy over the wide operating range and other features make the LMT87 an excellent alternative to thermistors.

For more details on this device, refer the LMT87 product page.

2.2.13 TL431

The TL431 is three-terminal adjustable shunt regulators, with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between Vref (approximately 2.5 V) and 36 V, with two external resistors. These devices have a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications, such as onboard regulation, adjustable power supplies, and switching power supplies.

For more details on this device, refer the TL431 product page.

2.2.14 LMV762

The LMV76x devices are precision comparators intended for applications requiring low noise and low input offset voltage. The LMV761 single has a shutdown pin that can be used to disable the device and reduce the supply current. These devices feature a CMOS input and push-pull output stage. The push-pull output stage eliminates the need for an external pullup resistor. The LMV76x are designed to meet the demands of small size, low power and high performance required by portable and battery-operated electronics. The input offset voltage has a typical value of 200 µV at room temperature and a 1-mV limit over temperature.

For more details on this device, refer the LMV762 product page.

2.2.15 TMS320F280049 C2000 MCU

The Piccolo™ TMS320F28004x (F28004x) is a powerful 32-bit floating-point microcontroller unit (MCU) that lets designers incorporate crucial control peripherals, differentiated analog, and nonvolatile memory on a single device. The real-time control subsystem is based on TI's 32-bit C28x CPU, which provides 100 MHz of signal processing performance. The C28x CPU is further boosted by the new TMU extended instruction set, which enables fast execution of algorithms with trigonometric operations commonly found in transforms and torque loop calculations; and the VCU-I extended instruction set, which reduces the latency for complex math operations commonly found in encoded applications. The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and it can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching. The F28004x supports up to 256KB (128KW) of flash memory divided into two 128KB (64KW) banks, which enables programming and execution in parallel. Up to 100KB (50KW) of on-chip SRAM is also available in blocks of 4KB (2KW) and 16KB (8KW) for efficient system partitioning. Flash ECC, SRAM ECC/parity, and dual-zone security are also supported. High-performance analog blocks are integrated on the F28004x MCU to further enable system consolidation. Three separate 12-bit ADCs provide precise and efficient management of multiple analog signals, which ultimately boosts system throughput. Seven PGAs on the analog front end enable on-chip voltage scaling before conversion. Seven analog comparator modules provide continuous monitoring of input voltage levels for trip conditions. The TMS320C2000™ devices contain industry-leading control peripherals with frequency-independent ePWM/HRPWM and eCAP allow for a best-in-class level of control to the system. The built-in 4-channel SDFM allows for seamless integration of an oversampling sigma-delta modulator across an isolation barrier.

For more details on the product, refer the TMS320F280049 product page.

2.2.16 TMDSCNCD280049C

TMDSCNCD280049C is an HSEC180 controlCARD based evaluation and development tool for the C2000™ Piccolo F28004x series of microcontroller products. controlCARDs are ideal to use for initial evaluation and system prototyping.

For more details on the product, refer the TMDSCND280049C product page.

2.3 System Design Theory

The following sections give an extensive overview of the operating principles of the dual-active bridge.

2.3.1 Dual Active Bridge Analogy With Power Systems

Power transfer between the two bridges in a dual-active bridge is analogous to the power flow between two voltage buses in a power system. Consider two voltage sources connected by a line reactance as shown in Figure 2-2.
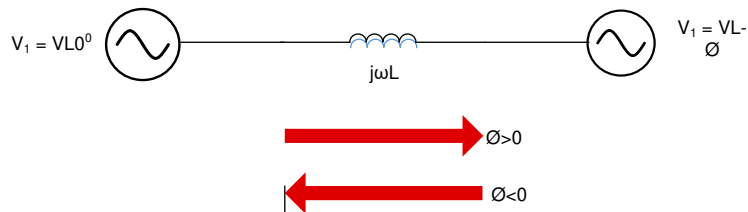

$V_1 = VL0^0$ $j\omega L$ $V_1 = VL-\emptyset$

$\emptyset > 0$

$\emptyset < 0$

Figure 2-2. Power Transfer Between Voltage Bus

Figure 2-2 shows that the voltage source on the right is lagging with respect to the voltage source on the left. Hence, the power transfer takes place from the left towards the right as per Equation 1.

$$P = \frac{V1 \times V2 \times \sin\emptyset}{\omega \times L}$$

(1)

Similarly, power transfer happens in a dual-active bridge where two high-frequency square waves are created in the primary and secondary side of the transformer by the switching action of MOSFETs. These high-frequency square waves are phase shifted with respect to each other. Power transfer takes place from the leading bridge to the lagging bridge, and this power flow direction can be easily changed by reversing the phase shift between the two bridges. Hence, it is possible to obtain bidirectional power transfer with ease in a dual-active bridge as shown in Figure 2-3.
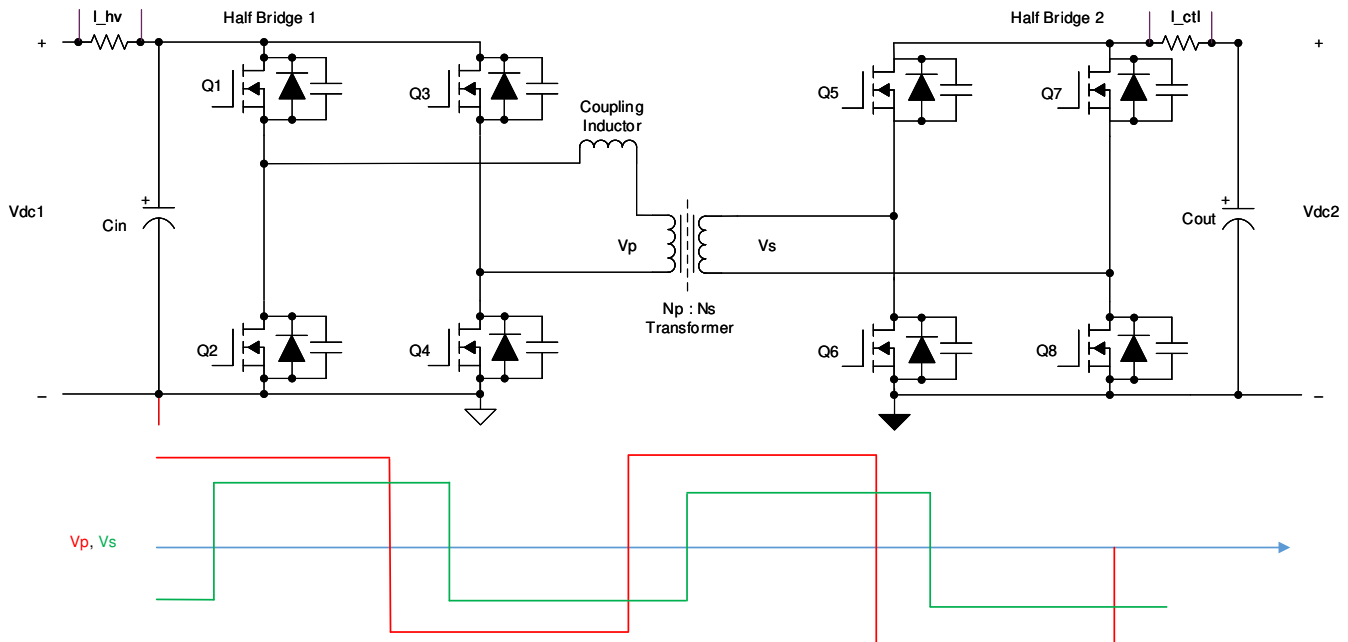
Figure 2-3. Dual-Active Bridge

2.3.2 Dual-Active Bridge - Switching Sequence

In a single-phase, dual-active bridge, primary and secondary bridges are controlled simultaneously. All switches operate at 50% duty ratio. The diagonal switches turn on and turn off together so that the output of each bridge is a square wave. The switching sequence of the converter is elaborated in detail in this section.

The switching sequence is divided into four intervals based on the inductor current waveform and phase shift between the voltages at the primary and secondary of the transformer. The voltage and the current waveforms are depicted in Figure 2-10. During interval one, the inductor current waveform is both positive and negative, and hence, the current commutation follows the scheme shown in Figure 2-4 and Figure 2-5. During this interval, switches Q1 and Q4 in the primary and switches Q6 and Q7 in the secondary conduct current.
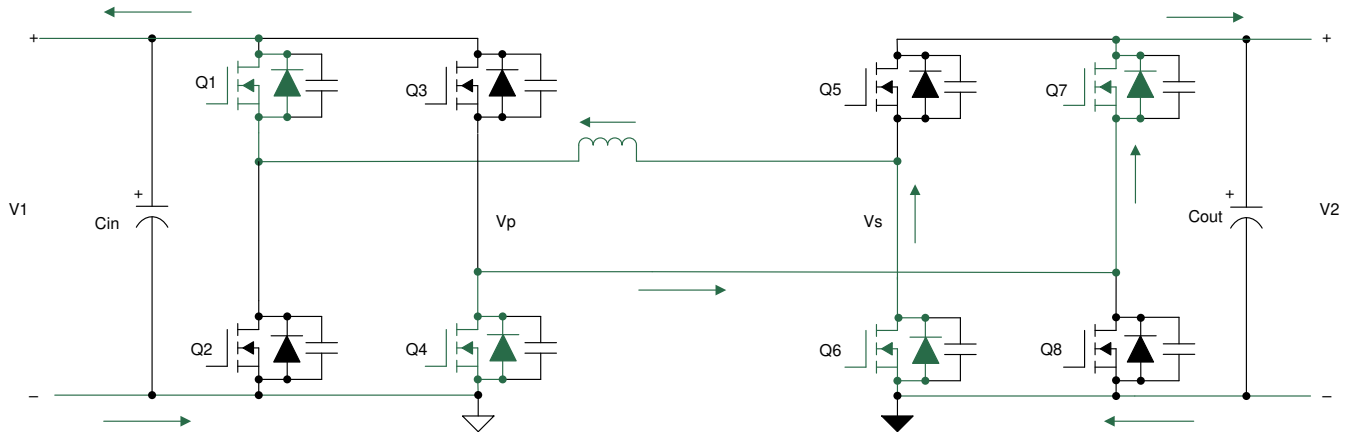
Figure 2-4. Interval 1: Negative Inductor Current
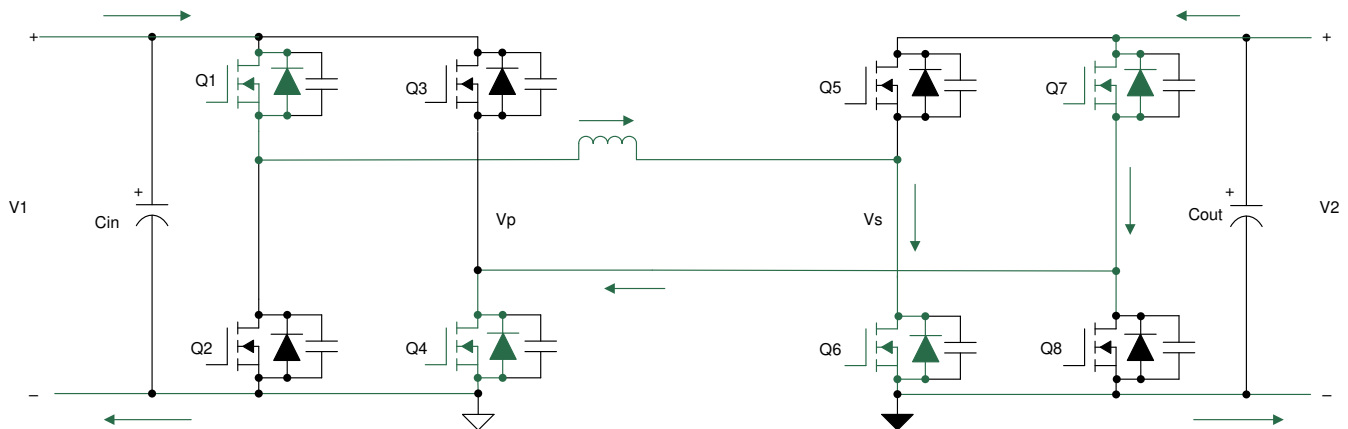
Figure 2-5. Interval 1: Positive Inductor Current

During this interval, the voltage across the primary, Vp, is equal to V1, and the voltage across the secondary, Vs, is equal to V2. The difference between these voltages appears across the leakage inductor, and the slope of the current during this interval can be approximated by Equation 2.

$$\frac{di}{dt} = \frac{V1 + V2}{L}$$

(2)

During interval two, the inductor current is positive. The voltage across the transformer primary is positive and is equal to V1, and the voltage across the secondary winding is positive and is equal to V2. Hence, the difference of these two voltages appears across the leakage inductor, and the slope of the rising current during this interval can be calculated by Equation 3.

$$\frac{di}{dt} = \frac{V1 - V2}{L}$$

(3)

During this interval, switches Q1 and Q4 remain turned on, but as the voltage across the secondary is now V2 with the inductor current positive, switches Q5 and Q8 turn on to conduct current. There is a small dead time period between the turn off of Q6 and Q7 and the turn on of Q5 and Q8. During this dead time, the phenomenon of zero voltage switching (ZVS) occurs, which is explained in detail in the following section. The commutation sequence for the second interval is shown in Figure 2-6.
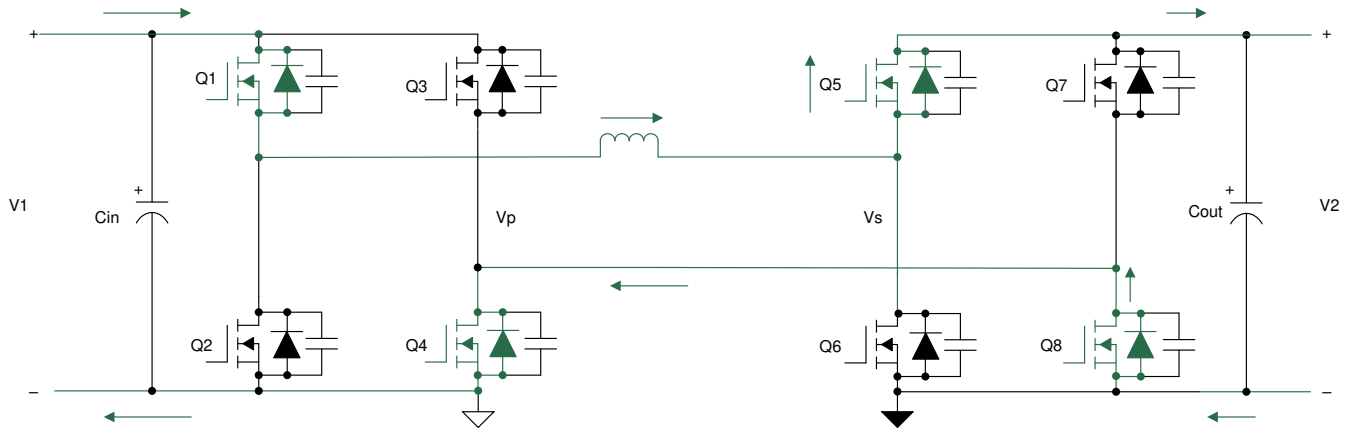
Figure 2-6. Interval 2

During interval three, the inductor current starts ramping down from its positive peak to a negative value as shown in Figure 2-10. In this interval, the voltage across the primary is –V1, and the voltage across the secondary is V2. The difference of these voltages, which is (-V1-V2), appears across the inductor. Hence, the current ramps down with a negative slope as shown in Equation 4.

$$\frac{di}{dt} = -\frac{V1 + V2}{L}$$

(4)

During this interval, switches Q5 and Q8 continue to remain turned on, but as the voltage across the primary is now –V1, switches Q2 and Q3 turn on to conduct current. The conduction for both directions of inductor current IL > 0 and IL < 0 is shown in Figure 2-7 and Figure 2-8 respectively.
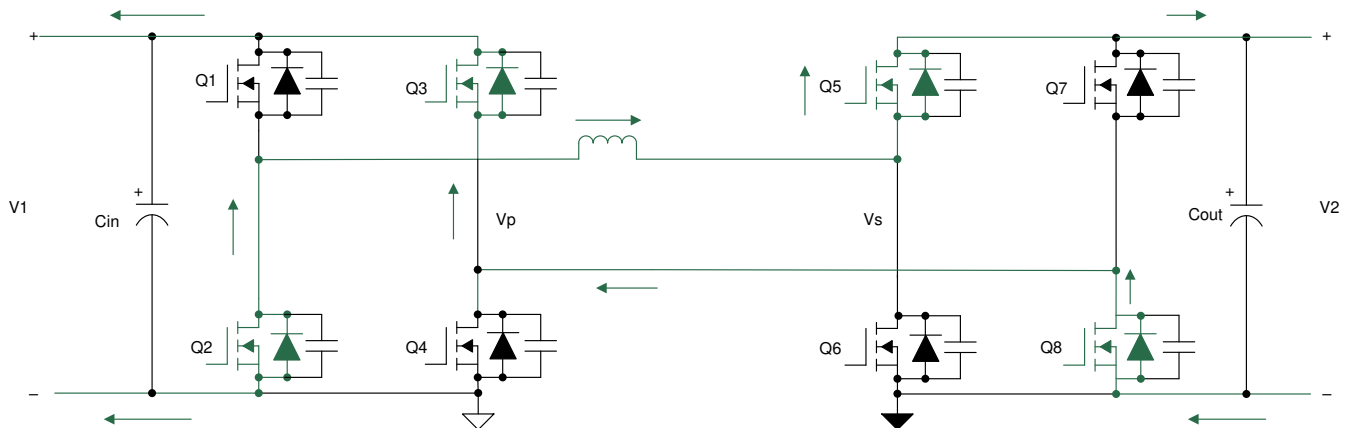
Figure 2-7. Interval 3: Positive Inductor Current
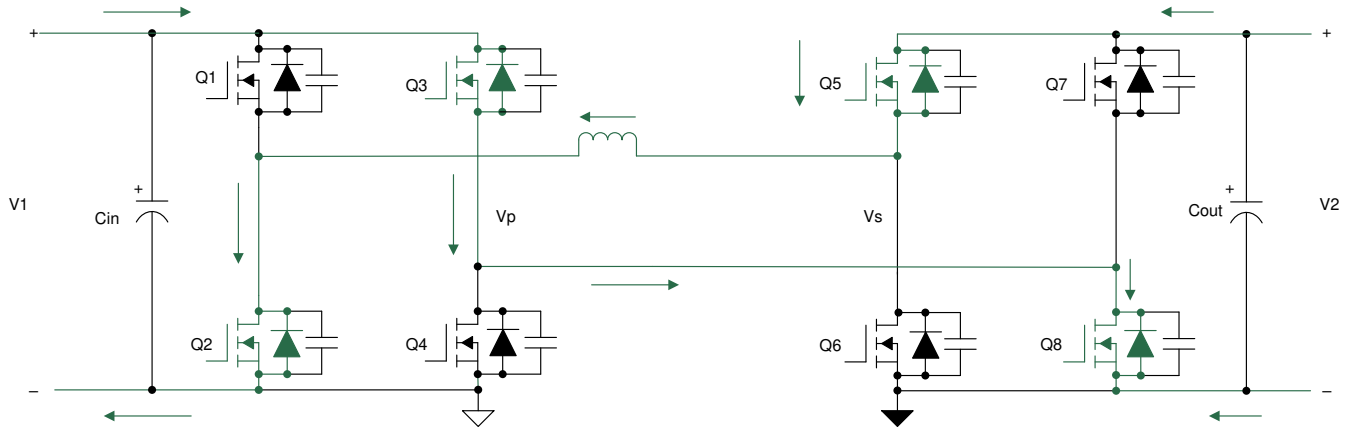
Figure 2-8. Interval 3: Negative Inductor Current

During interval four, the inductor current continues to be negative. During this interval, the voltage across the primary is –V1 and, and the voltage across the secondary is -V2. The difference in these voltages, which is (-V1+V2), appears across the inductor. Hence, the current ramps down with a negative slope as shown in Equation 5.

$$\frac{di}{dt} = -\frac{V1 - V2}{L}$$

(5)

During this interval, switches Q2 and Q3 continue to remain turned on, but as the voltage across the secondary are now –V2, switches Q6 and Q7 turn on to conduct current as shown in Figure 2-9.
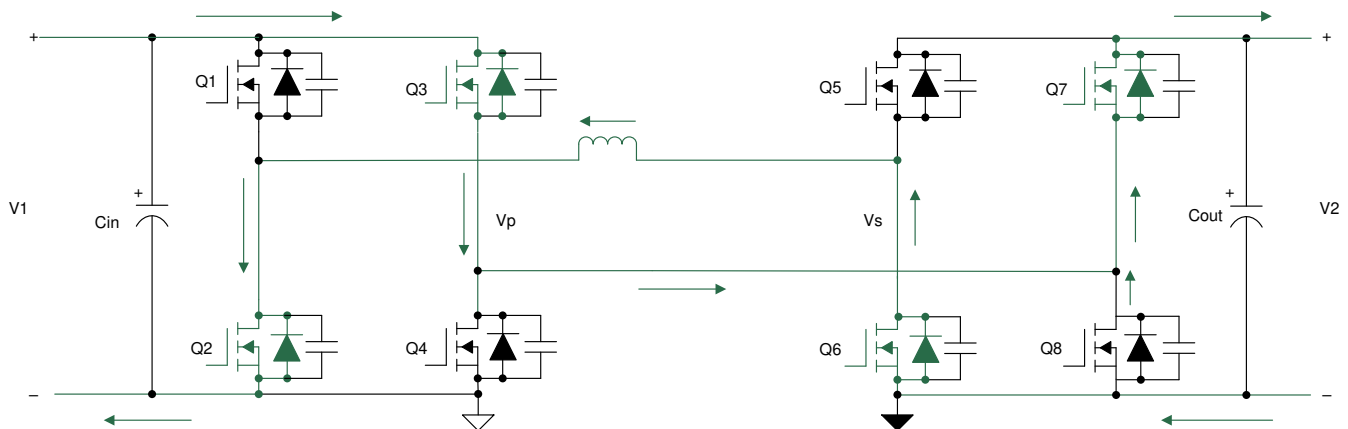
Figure 2-9. Interval 4

Figure 2-10 shows the gating pulses of the switches on the primary and secondary side. The variable Ø represents the phase shift between the PWM pulses of the primary and secondary side. Vp and Vs represent the voltage on the primary and secondary winding of the transformer. IL represents the transformer current.
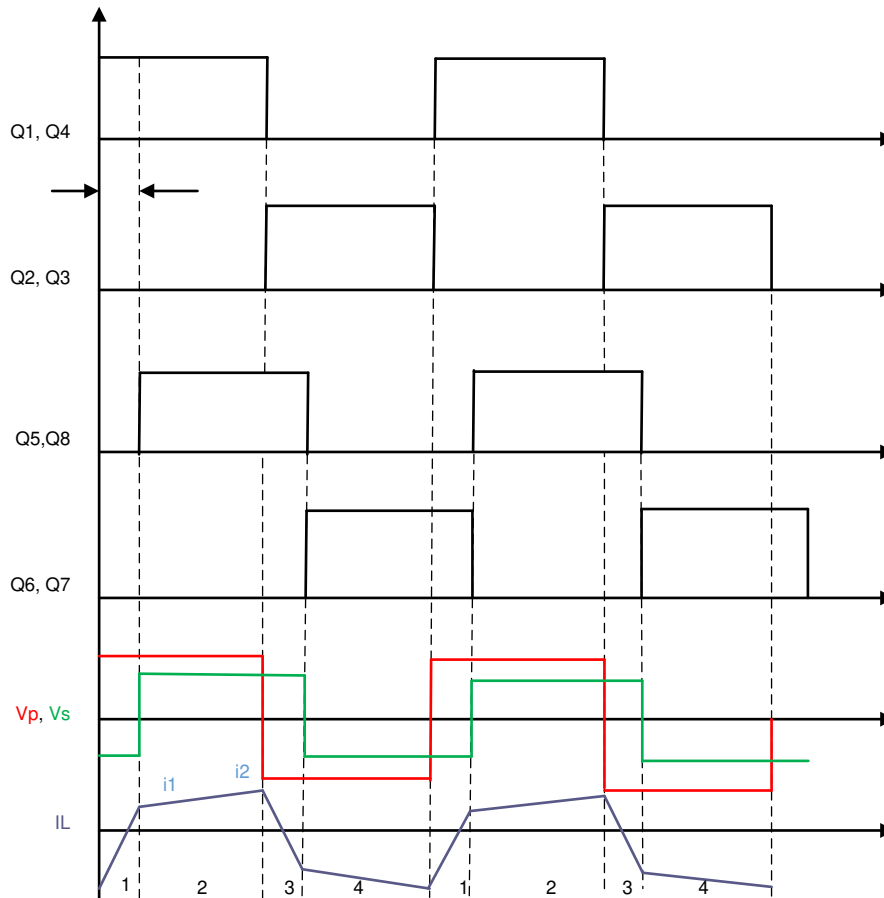
Figure 2-10. Gate Signals, Transformer Primary and Secondary Voltages, and Inductor Current

2.3.3 Dual-Active Bridge - Zero Voltage Switching (ZVS)

During the transition from interval one to two, there exists a small dead time where the inductor-stored energy discharges the output capacitances of the MOSFETs and holds them close to zero voltage before they are turned on. This phenomenon, where the voltage across the MOSFET is close to zero at turn on, is referred to as zero voltage switching (ZVS). This is a major advantage with this topology, where due to the natural lagging current in one of the bridges, the inductive stored energy causes ZVS of all of the lagging bridge switches and some of the switches of the leading bridge. This depends on the stored inductive energy ($E_L = 0.5LI^2$) available to charge and discharge the output capacitances of MOSFETs ($E_C = 0.5CV^2$).

When transition happens from interval one to two, the primary side switches Q_1 and Q_5 continue conduction, whereas in the secondary, Q_6 and Q_7 turn off and Q_5 and Q_8 turn on. Initially the voltage across Q_6 and Q_7 is zero when they are conducting, and Q_5 and Q_8 block the entire secondary voltage. During dead time, when all of the switches in the secondary are off, the inductor-stored energy circulates current which discharges the capacitor across MOSFETs Q_5 and Q_8 to zero and charges the capacitor across MOSFETs Q_6 and Q_7 to the full secondary voltage. The current commutation is shown in Figure 2-11.
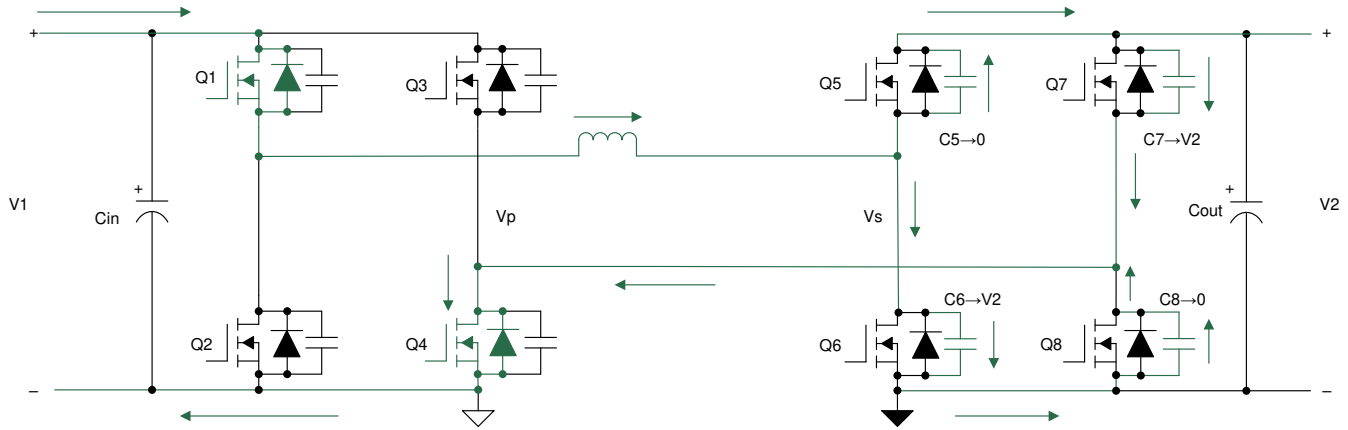
Figure 2-11. ZVS Transition in Secondary Side - Capacitor

Once the capacitors have been charged and discharged, the current must continue to flow. The current will flow through the diodes D_5 and D_8, thereby clamping the voltage across MOSFETs Q_5 and Q8 to zero as shown in Figure 2-12. During the next interval, MOSFETs Q_5 and Q_8 are turned on at zero voltage, thereby reducing turn on losses completely. The arrow close to the diode indicates that the diode is conducting and the MOSFET is off.
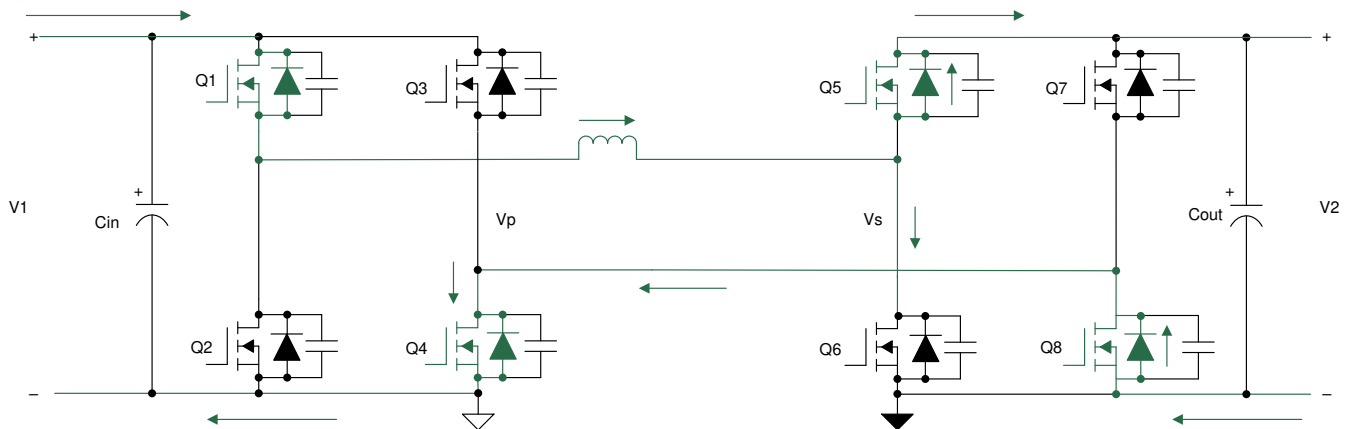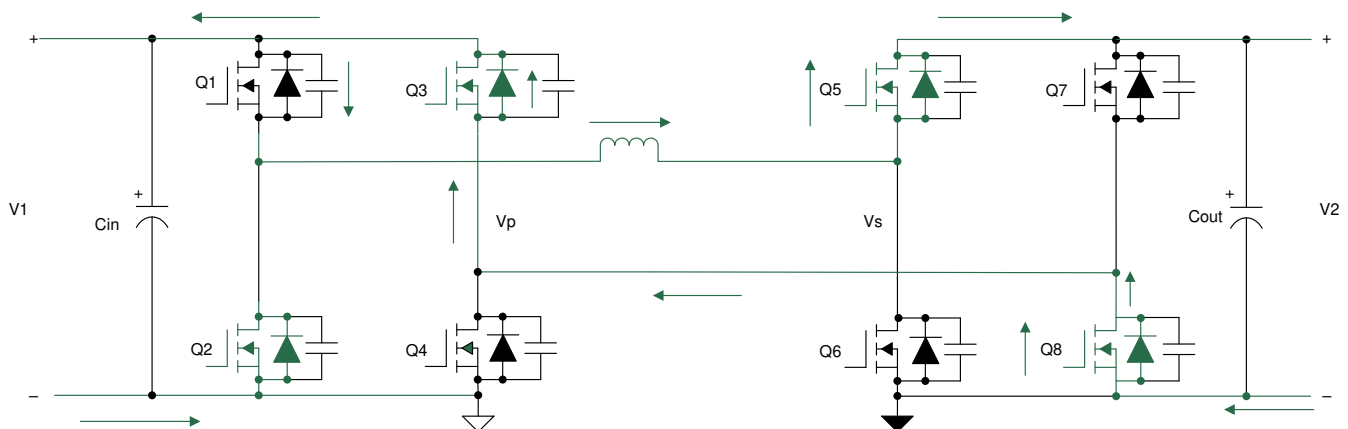

Figure 2-12. ZVS Transition in Secondary Side - Diode

Similarly, zero voltage switching across the switches of the primary during the transition from interval 2 to 3 is explained in the following section. When transition happens from interval two to three, the secondary side switches Q_5 and Q_8 continue conduction, whereas in the primary, Q_1 and Q_4 turn off and Q_2 and Q_3 turn on. Initially, the voltage across Q_1 and Q_4 is zero when they are conducting, and Q_2 and Q_3 block the entire secondary voltage. During dead time when all of the switches in the primary are off, the inductor stored energy circulates current, which discharges the capacitor across MOSFETs Q_2 and Q_3 to zero and charges the capacitor across MOSFETs Q_1 and Q_4 to the full primary voltage. The current commutation is shown in Figure 2-13.
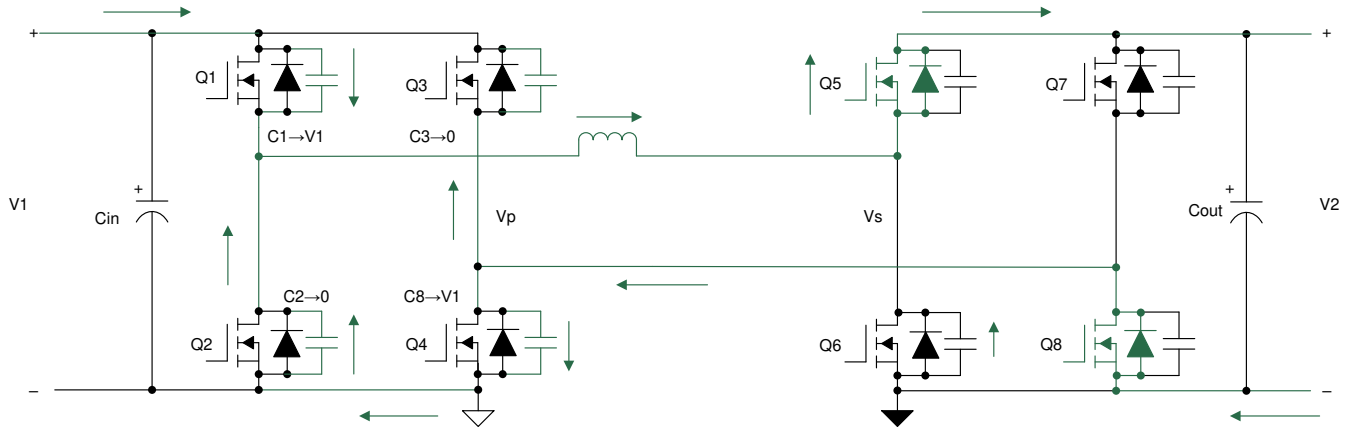
Figure 2-13. ZVS Transition in Primary Side - Capacitor

Once the capacitors have been charged and discharged, the current must continue to flow. The current will flow through diodes D2 and D3, thereby clamping the voltage across MOSFETs Q2 and Q3 to zero as shown in Figure 2-14. During the next interval, MOSFETs Q2 and Q3 are turned on at zero voltage, thereby reducing turn on losses completely. The arrow close to the diode indicates that the diode is conducting and the MOSFET is off.

Figure 2-14. ZVS Transition in Primary Side - Diode

2.3.4 Dual-Active Bridge - Design Considerations

A number of factors are critical in the design of the power stage of a dual-active bridge. The most important factors are the selection of leakage inductor, desired phase shift of operation, output capacitor rating, switching frequency of operation, selection of SiC MOSFETs, transformer, and intended ZVS range of operation. Many of these design parameters are interrelated, and selection of any one of them has a direct impact on the others. For example, the selection of leakage inductor has a direct effect on the maximum power transferred, which in turn affects the phase shift of operation of the converter at the intended power level. Each of these factors are discussed in detail in the following sections.

2.3.4.1 Leakage Inductor

The most important design parameter is the selection of leakage inductor. The power transfer relation of the dual-active bridge is given by Equation 6.

$$P = \frac{nV_1V_2\varnothing(\pi - \varnothing)}{2\pi^2F_SL}$$

(6)

Equation 6 shows that a low value of inductance will lead to high power transfer capability. The maximum value of power transfer for a given switching frequency, leakage inductor, and input and output voltage will occur at $\varnothing = \pi/2$.

Figure 2-15 shows the inductor current waveform. The value of current at points i_1 and i_2 can be derived from this waveform.

$$i_1 = 0.5\left(2d\emptyset + (1-d)\pi\right)I_{nom} \tag{7}$$

$$i_2 = 0.5\left(2\emptyset - (1-d)\pi\right)I_{nom} \tag{8}$$

Where d is the voltage transfer ratio of the converter given in Equation 9 and I_{nom} is the nominal base current of the converter.
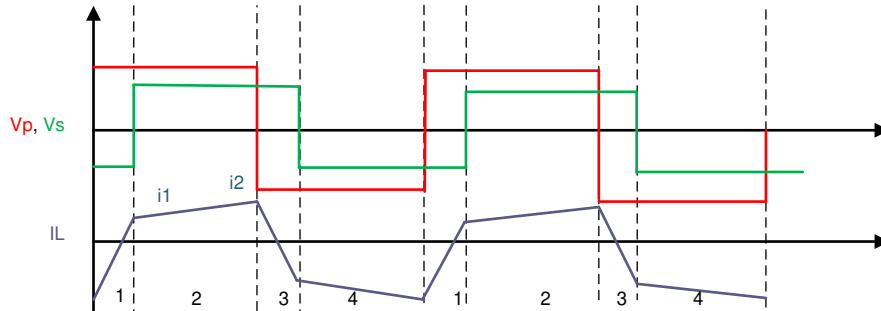
$$d = \frac{V_2}{NV_1} \tag{9}$$

Figure 2-15. Inductor Current Waveform

From Equation 7 and Equation 8, the conditions for zero voltage switching for leading and lagging bridge of the converter can be obtained.

From the following conditions, the conditions for ZVS are obtained in terms of phase and voltage gain of the converter, summarized in Equation 10 and Equation 11 for the primary bridge and secondary bridges respectively.

- $i_1 > 0$ for the secondary side bridge
- $i_2 > 0$ for the primary side bridge

$$\emptyset > \left(1 - \frac{1}{d}\right)\pi/2 \tag{10}$$

$$\emptyset > (1-d)\pi/2 \tag{11}$$

By combining Equation 7, Equation 8, Equation 10, and Equation 11, the relationship between output power and voltage ratio for different values of the inductor is obtained. A MATLAB® script used to plot this relationship is depicted in Figure 2-16. The figure shows that for a particular value of inductance, when the voltage transfer ratio changes from unity, the converter switches experience hard switching. As long as the voltage transfer ratio is kept at unity, soft switching across both the primary and secondary leg switches is obtained. The most important point to note is that the soft switching region (zero voltage switching) depends on the value of leakage inductance. As the value of inductance increases, the ability for soft switching of the converter extends up to very low power levels (light loads).
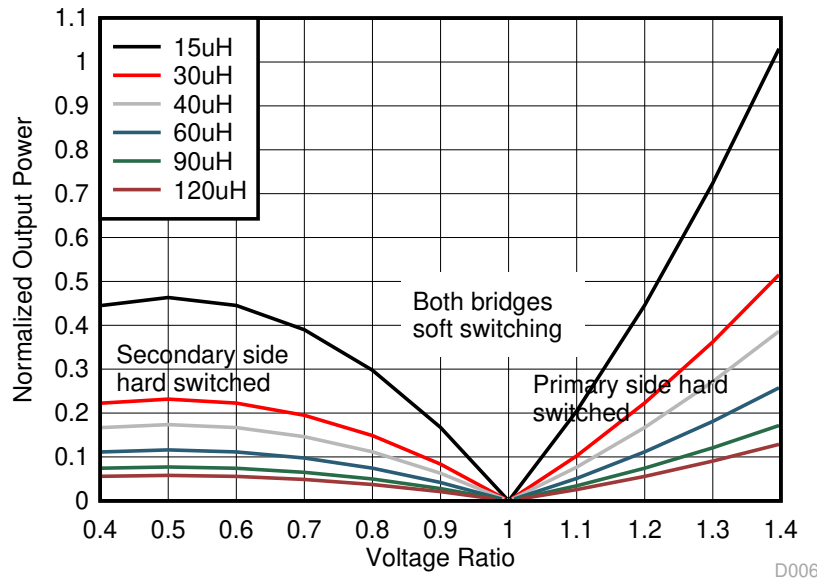
Figure 2-16. ZVS Range and Output Power Versus Voltage Transfer Ratio

2.3.4.2 Effect of Inductance on Current

In the previous section, it is noted that a high value of leakage inductance can contribute to soft switching up to a very low power level and hence leads to better switching performance. Alternatively, increasing the leakage inductance leads to increased RMS currents in the primary and secondary of transformer, switch currents, and ripple currents in the capacitor as described in the following sections. Equation 12 and Equation 13 show the RMS currents across the primary and secondary side.

$$I_{P\_rms}^2 = i_1^2 + i_2^2 + i_1 i_2 \frac{1 - 2\frac{\varnothing}{\pi}}{3} \tag{12}$$

$$I_{S\_rms} = \frac{Np}{Ns} I_{P_{rms}} \tag{13}$$

Using these equations and the equation for power transfer, the variation in current across the primary and secondary side with inductance is plotted in Figure 2-17.
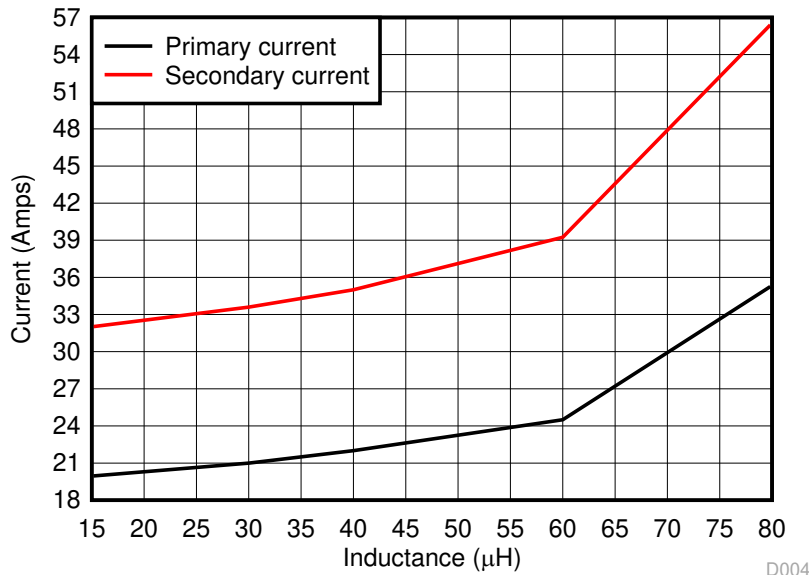
Figure 2-17. Variation of RMS Currents With Leakage Inductance

Figure 2-17 shows that as the value of leakage inductance increases, the RMS currents in the transformer and switches increase, leading to more conduction losses. Thus, there exists a tradeoff between an optimal value of leakage inductance to affect ZVS and minimizing conduction losses.

2.3.4.3 Phase Shift

The phase shift of the converter is dependent on the value leakage inductor. The phase shift for required power transfer is given by Equation 14.

$$\varnothing = \frac{\pi}{2} \times \left(1 - \sqrt{1 - \frac{8 \times F_s \times L \times P_{out}}{n \times V_1 \times V_2}} \right) \tag{14}$$
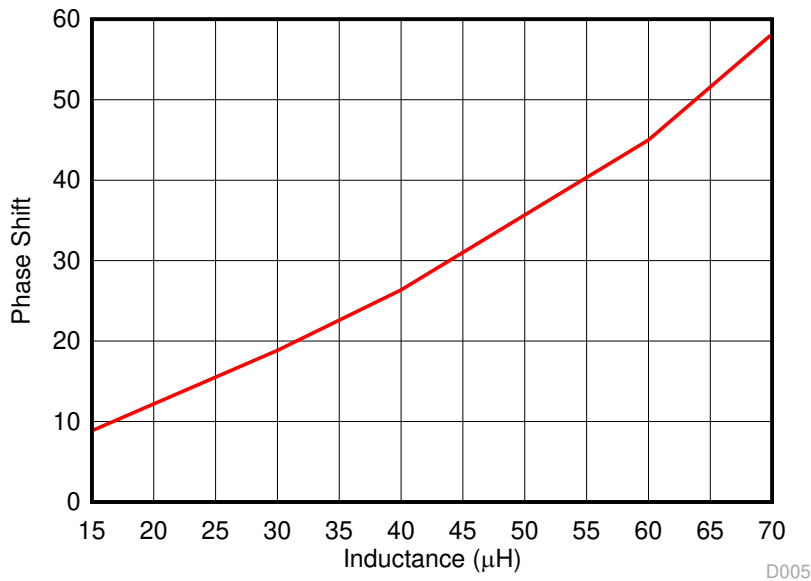
Figure 2-18. Variation of Phase Shift With Leakage Inductance

Figure 2-18 shows that for a small value of inductance, a maximum power transfer at a small value of phase shift is obtained. To have fine control over power transferred, fine high resolution steps in which the phase can be varied must be obtained. Alternatively, a larger inductor can obtain maximum power transfer at a high value of phase shift for better control.

2.3.4.4 Capacitor Selection

The output capacitor in the dual-active bridge must be designed to handle the ripple. This value impacts the output voltage specification. From Figure 2-19, Equation 15 and Equation 16 are obtained.

$$I_{cap} = I_{hb2} - I_{load} \tag{15}$$

$$C\frac{dV_2}{dt} = \frac{V_1}{X_L}\varnothing\left(1 - \frac{\varnothing}{\pi}\right) - \frac{V_2}{R} \tag{16}$$
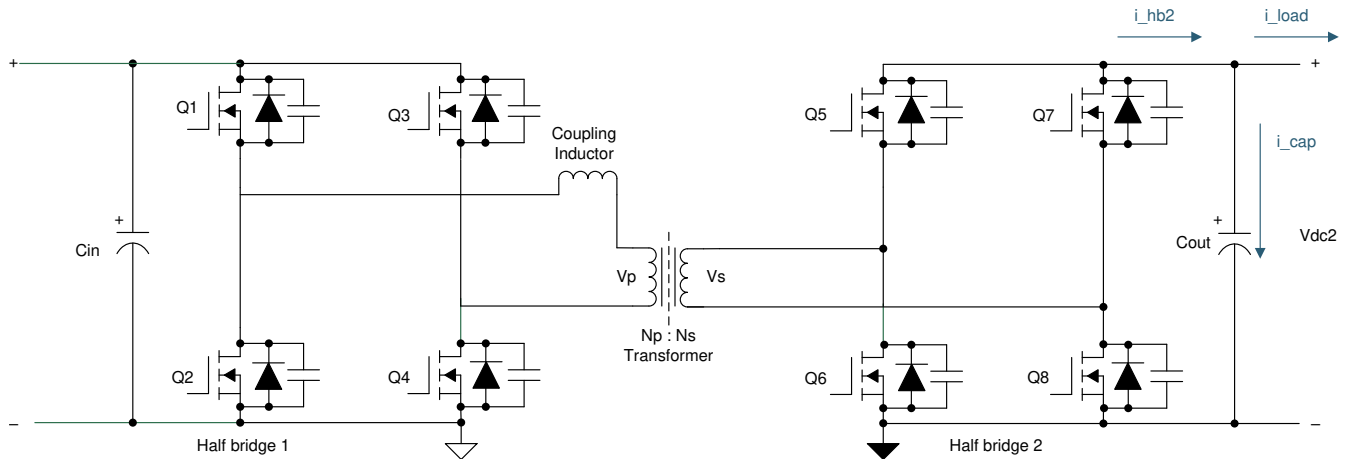
Figure 2-19. Output Current in Dual-Active Bridge

Figure 2-20 shows the effect of the leakage inductor on the selection of the output capacitance. For a particular value of phase shift and inductance, capacitance required for containing the voltage ripple to a specified limit, as per the system specification, increases as the leakage inductor increases. This also means that more capacitance is needed to handle the voltage ripple. As the RMS value of capacitor current increases, more is the loss dissipated across the equivalent series resistance (ESR) of capacitance. Considering these factors, the output capacitor was chosen to keep the output voltage under 5% ripple.
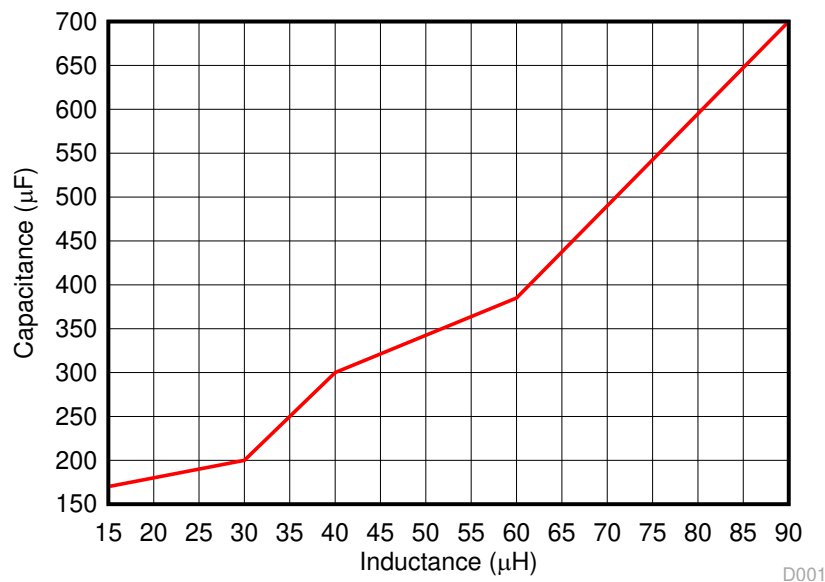
Figure 2-20. Desired Output Capacitance Versus Leakage Inductance

2.3.4.5 Soft Switching Range

Figure 2-16 shows that the soft switching range of the converter is maximized when the turns ratio is chosen such that the primary voltage is equal to the reflected secondary voltage. In this condition, the voltage transfer ratio is equal to unity, and all of the switches of the primary and secondary side experience soft switching under all conditions. In practice, the total capacitance of the switching node must be discharged by currents i1 and i2 as given by Equation 7 and Equation 8 within the specified dead time so that switches turn on at zero voltage. For light load conditions where there is not sufficient inductive stored energy to discharge the capacitive energy of the MOSFETs, the dead time could be increased in accordance with current so as to affect ZVS.

2.3.4.6 Switching Frequency

Switching frequency is another important design parameter which affects the efficiency and power density of power converter. The input and the output voltage levels primarily determine the type of switches used in the power stage. Usage of SiC MOSFETs in the power stage drives the switching frequencies to very high

levels. Operating at higher switching frequencies enables reduced size of magnetics which help in improved thermal solution, thereby improving power density of the converter. Therefore, selection of switching frequency is primarily a tradeoff between the allowable heat sink solution and transformer size for a given efficiency target. Secondly, if the output capacitance (Ecoss) of MOSFET is very high, selection of high switching frequency leads to high switching losses at light load and hampers efficiency. Selection of switching frequency also affects the control loop bandwidth implementation. Considering all of these parameters, 100 kHz was used as the switching frequency for this application.

2.3.4.7 Transformer Selection

In a power supply design, transformers and inductors are major contributors to size. Increasing the operating frequency reduces their size, but increasing the switching frequency beyond a particular value affects the efficiency of the power module. This is because the skin effect becomes very high at that frequency where the current flows through the surface of the conductor. Similar to the skin effect, there is a proximity effect, which causes current to only flow on surfaces closest to each other. Furthermore, from a proximity standpoint in high-frequency designs, conductor size and the number of layers must be optimized. With a planar transformer, more interleaving to reduce the proximity effect can be achieved. This interleaving can be tailored to produce a specific amount of leakage so as to aid in power transfer and to contribute to ZVS.

Planar transformers offer the following advantages over conventional transformers and hence were used in this reference design:

- Planar magnetics have very high power density. They are more compact and consume less space when compared to a conventional transformer of the same power rating.
- They have the ability to do more interleaving to reduce AC conductor losses.
- They have consistent spacing between turns and layers which translate into consistent parasitics. Both leakage inductance and intra-winding capacitances can be maintained to very predictable and tight values.
- Tight control over the leakage inductance is possible with planar magnetics.
- The transformer's compact size can support integration of the additional shim inductor with the transformer itself without the need for a separate component on board.

focuses on the actual planar transformer chosen for this application with details on the loss numbers.

The leakage inductor alone cannot ensure soft switching up to light loads. As seen previously, increasing the soft switching range by increasing inductor value increases the RMS currents. In practice, leakage inductor is chosen to provide soft switching only up to ½ or 1/3 of rated load. Beyond this point, the transformer magnetizing inductance is used for ensuring soft switching near light loads. The magnetizing inductance is chosen generally ten times the value of leakage inductance as a starting point for this optimization.

2.3.4.8 SiC MOSFET Selection

As shown in Figure 2-1, the main power stage switching devices of the primary and secondary must block the full input and output DC voltages. SiC switches were chosen for the following reasons:

- The switching speed of the SiC MOSFET is faster than a traditional Si device, thereby reducing switching losses.
- The reverse recovery charge is significantly smaller in the SiC MOSFET for DAB application, resulting in reduced voltage and current overshoot.
- Lower state resistance will significantly reduce conduction losses during on time of the device.
- The switches have the ability to block higher voltages without breaking down.

For this design, 1200-V Cree® devices with on state resistance of 16 mΩ were used on the primary side, and a 900-V, voltage-blocking Cree device with on state resistance of 30 mΩ was used in the secondary. Both are four-pin devices with a kelvin connection for better switching performance. The actual conduction and switching loss calculations are shown in the following sections.

2.3.5 Loss Analysis

In this section, the theoretical efficiency numbers obtained in the dual-active bridge are reviewed. To arrive at the losses in different elements, the average and the RMS currents across the primary and secondary side are calculated. Details on the actual derivation of equations are out of scope for this design. The maximum power transfer in a dual-active bridge occurs at a phase shift of 90°. However, a high phase shift requires a high

leakage inductance for power transfer. Using a high inductor leads to increased RMS currents in the primary and secondary side, which affects the efficiency of the converter.

Figure 2-18 shows the relationship between phase shift and the required inductance obtained from MATLAB simulations. The system specifications are tabulated in Table 2-1.

Table 2-1. DC/DC Converter Electrical Parameters

Phase shift	$-0.44 < \text{Ø} < 0.44$ (rad)
Total Leakage Inductance	35 µH
Turns Ratio	1: 0.625
Load resistance	26 Ω
Input Voltage	800 V
Output voltage	500 V
Input current	12.5 A
Output current	20 A
Output Power	10 kW

2.3.5.1 Design Equations

The voltage transfer ratio, m, for a dual-active bridge is given by Equation 17, where N is the primary-to-secondary turns ratio.

$$m = \frac{V_o}{NV_{in}} \tag{17}$$

The required leakage inductor for phase shift is calculated from Equation 18.

$$L_{lk} = \text{Ø}\left(1 - \text{Ø}\right) NV_{in} \frac{V_{out}}{2F_{sw}P_{out}} = 36 \text{ µh} \tag{18}$$

For the required phase shift of 23°, the required leakage inductance calculated from this equation is approximately 36 µH. The total transformer leakage inductance is around 23 µH when referred to the output side. Hence, an additional shim inductance of between 13 µH to 15 µH is needed to achieve the required power transfer at this value of phase shift. This approximately matches the simulation results for required phase shift against inductance.

2.3.5.2 SiC MOSFET and Diode Losses

As SiC is used in the power stage, the body diodes conduct only during the dead time, causing ZVS. In all other instances, the channel of SiC is turned on to conduct current. The peak current in the primary is calculated using Equation 19. In this equation,

- Leakage inductance is 32 µH
- Phase shift is 23 degrees
- N is the primary-to-secondary turns ratio, which is 1.6
- n is secondary to primary turns ratio, which is 0.625

$$I_p = \frac{T_s}{2L_k}\left(nV_{in} + V_{out}\left(2\text{Ø} - 1\right)\right) = 22 \text{ A} \tag{19}$$

The RMS and average values of currents through current through the switches and diodes of the primary side are calculated using Equation 20 and Equation 21. In these equations, I_l is equal to I_p because duty cycle is operating at 0.5.

$$I_{switch\_prim\_rms} = \sqrt{\frac{1}{3T_S}\left(I_p^2(t_{zero}) + I_p^2\left(\emptyset\frac{T_s}{2} - t_{zero}\right) + \left(\frac{T_s}{2} - \emptyset\frac{T_s}{2}\right) \times \left(I_p^2 + I_l^2 + I_l I_p\right)\right)} = 15.65 \text{ A}$$

(20)

The RMS value of switch current is calculated from Figure 2-21 over a switching cycle. The diode conducts for only a small fraction of time during the switching period, as in, the dead time causing ZVS. The dead time chosen for this application is 200 ns.

$$I_{diode\_prim\_avg} = t_{dead\_time}\frac{I_p}{T_s} = 0.44 \text{ A}$$

(21)

From the data sheet of the SiC MOSFETs, the value of drain-source resistance corresponding to the applied gate voltage waveform is obtained. This value is approximately 20 mΩ. The forward voltage drop across the body diode is 4.2 V. The conduction losses across the four primary side FETs is calculated using Equation 22:

$$P_{cond\_prim} = 4\left(I_{switch\_prim\_rms}^2 R_{ds\_on\_prim} + I_{diode\_prim\_avg} V_{fd_{prim}}\right) = 27 \text{ W}$$

(22)

Similarly, the conduction losses are calculated across the secondary side FETs by scaling the primary side RMS currents with transformer turns ratio using Equation 23 and Equation 24. The on state resistance of the secondary side MOSFET is approximately 33 mΩ.

$$I_{switch\_sec\_rms} = N \times I_{switch\_prim\_rms} = 25 \text{ A}$$

(23)

$$P_{cond\_sec} = 4\left(I_{switch\_sec\_rms}^2 R_{ds\_on\_sec} + I_{diode\_avg\_sec} V_{fd\_sec}\right) = 95 \text{ W}$$

(24)
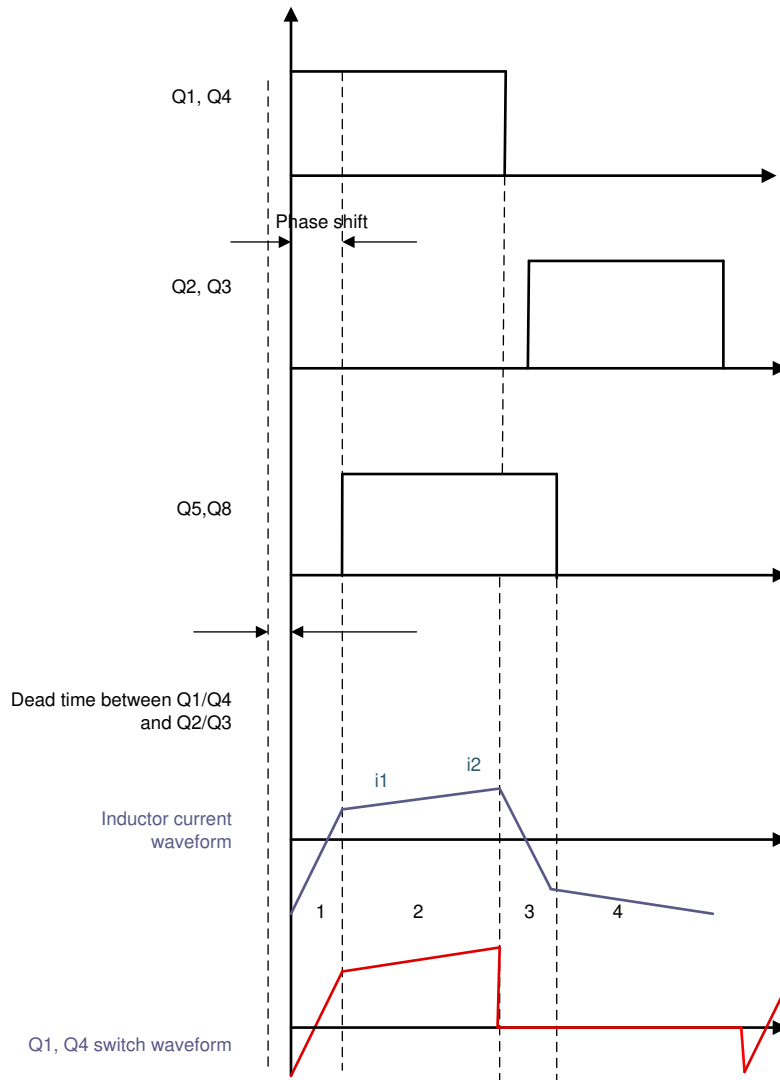
Figure 2-21. Switch Current Waveforms for Calculating RMS Value of Current

To calculate switching losses, the switching loss curves from the manufacturer are used. Shown in Figure 2-22 and Figure 2-23 are the switching loss curves from manufacturer for the primary and secondary side FETs.
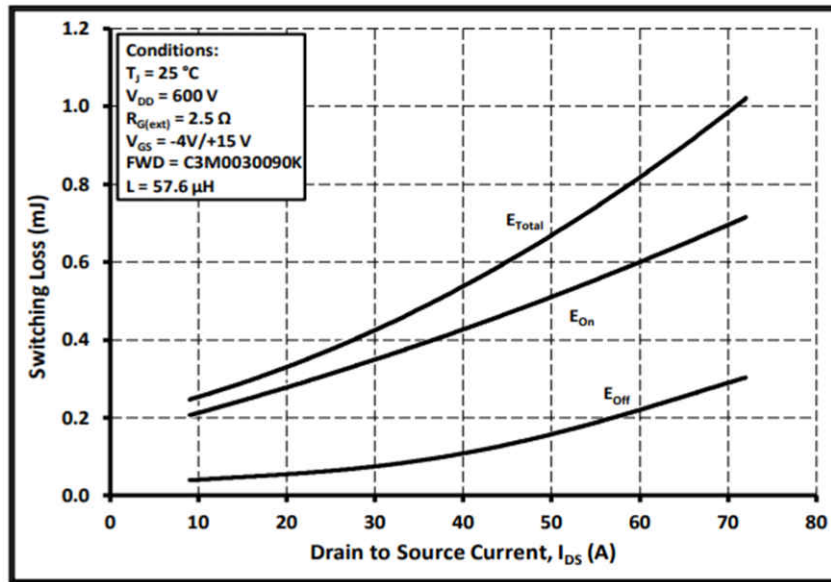
Figure 2-22. C3M0030090K Loss Curves
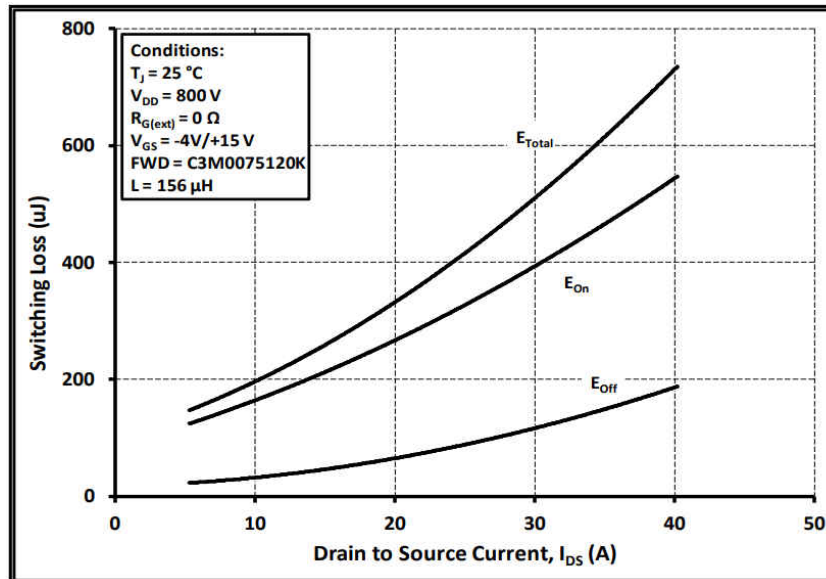
Figure 2-23. C3M0016120K Switching Curves

Because the FETs turn on at zero voltage, only the turn off loss coefficients are used for calculating the switching losses. Consider the secondary side MOSFETs for illustrating the calculation of switching losses. The curves are characterized during the double pulse test for a voltage of 600 V. From the graph, it can be inferred that at 50 A, the turn off energy is around 0.18 mJ. Using this information in Equation 25, the values of switching loss is obtained.

$$P_{sw\_turnoff\_sec} = \frac{F_s E_{off\_sec} I_{pk\_sec} V_{out}}{V_{nom} I_{nom} \pi} = 3.34 \text{ W}$$

(25)

In Equation 25, V_{out} is the maximum secondary voltage at 500 V, I_{pk_sec} is the maximum current in the secondary at approximately 35 A, F_s is the switching frequency, E_{off_sec} is the turn off loss coefficient, and V_{nom} and I_{nom} are obtained from the data sheet. Similarly, the turn off loss across the primary is calculated in Equation 26.

$$P_{sw\_turnoff\_prim} = \frac{F_s E_{off\_prim} I_{pk\_sec} V_{in}}{V_{nom} I_{nom} \pi} = 3.85 \text{ W}$$

(26)

Total turn off switching losses in the primary and secondary side across all eight switches comes to 36 W. In addition to these losses, two switches of the primary turn on at non-zero voltage, leading to switching losses during turn. This is because the inductor stored energy ($0.5 \, Li^2$) at this point is not fully sufficient to discharge the capacitive energy ($0.5 \, CV^2$) at the output of the MOSFETs. These losses are calculated in the same way as calculated previously, but the turn on loss coefficients are taken. These losses come to approximately 24 W across both of the switches.

$$P_{sw\_turnon\_prim\_nonZVS} = \frac{F_S E_{on\_prim} I_{pk\_prim} V_{in}}{V_{non} I_{nom} \pi} = 6.13 \text{ W}$$

(27)

2.3.5.3 Transformer Losses

This section provides an estimate of the different components of transformer loss. The transformer for this design was completed with the help of Payton Planar Magnetics®. This reference design focuses only on the loss of numbers and not the actual design process of the transformer. To select the core for this transformer, the area product approach is considered. The area product of the transformer is calculated by Equation 28.

$$A_p = \frac{\left(V_1 \times I_{1.avg} + V2 \times I_{2.avg}\right) \times 10^4}{k_f \times k_u \times F_{SW} \times B_m \times J} = 14.067 \text{ cm}^4$$

(28)

where

- k_f is the waveform factor
- k_u is the utilization factor
- F_{SW} is the switching frequency
- B_m is the maximum flux density
- J is the current density
- V_1 is the primary voltage
- $I_{1.avg}$ is the primary average current
- V_2 is the secondary voltage
- $I_{2.avg}$ is the secondary average current

Substitute the values for flux density as 0.2 T, switching frequency as 100 kHz, and utilization factor as 0.3 as this is a planar design. With a waveform factor of 4 and current density as 400 A/cm^2, the area product is calculated as 18 cm^4. Choosing a core with area product greater than the calculated value, E64/18/50 ferrite DMR44 core was chosen.

Next, the number of turns required for the primary and secondary side is calculated. The number of primary turns is calculated using Equation 29.

$$N_p = \frac{V_{in} 10^4}{K_f B_m A_e F_{sw}} = 22$$

(29)

From the data sheet for the core, the effective core area, A_e, is 516 mm^2. By substituting this value, the number of turns is approximately 22. In a practical implementation, the number of turns selected in the primary was 24. By using the required conversion ratio of 1.6 between the primary and secondary, the number of secondary turns, N_s, is 15 turns.

Figure 2-24 shows the parameters of the core obtained from the data sheet. The core loss per unit of volume, P_v, at 100°C is approximately 300 mW/cm^3. The core volume, A_e, is 81.9 cm^2. Therefore, the total core loss at 100 kHz is given by Equation 30.

$$P_{Core\_loss} = P_v \, A_e = 24 \, W$$

(30)

DMR44材料特性・DMR44 Material Characteristics

特性 SYMBOL	测试条件 CONDITIONS		典型值 VALUE
初始磁导率 μi Initial permeability	10kHz, B<0.25mT	25℃	2400 ± 25%
饱和磁通密度 Bs (mT) Saturation flux density	50Hz, 1194A/m	25℃	510
		100℃	400
剩磁 Br(mT) Residual magnetic flux density		25℃	110
		100℃	60
矫顽力 Hc(A/m) Coercive force		25℃	15
		100℃	6
功耗 Pv(mW/cm³) Power loss	100kHz, 200mT	25℃	600
		60℃	400
		100℃	300
		120℃	380
居里温度 Tc (℃) Curie temperature	10kHz, B<0.25mT		>215
电阻率 ρ (Ω・m) Resistivity		25℃	2.0
密度 d(g/cm³) Density		25℃	4.8

Figure 2-24. Transformer Core Data

From the data sheet of the manufacturer, the primary and secondary winding DC resistances were 43 mΩ and 16 mΩ, respectively. The copper losses in the windings were calculated as per Equation 31.

$$P_{Copper} = I_{prim\_rms}^2 \, R_{dc\_prim} + I_{sec\_rms}^2 \, R_{dc\_sec} = 20.5 \, W$$

(31)

Losses due to the AC resistance at high frequencies are also arising as a result of the skin effect. At 100 kHz, Figure 2-25 shows that the AC resistance is approximately 12.5 mΩ. These contribute 8 W of loss due to current flowing in the primary and secondary windings.
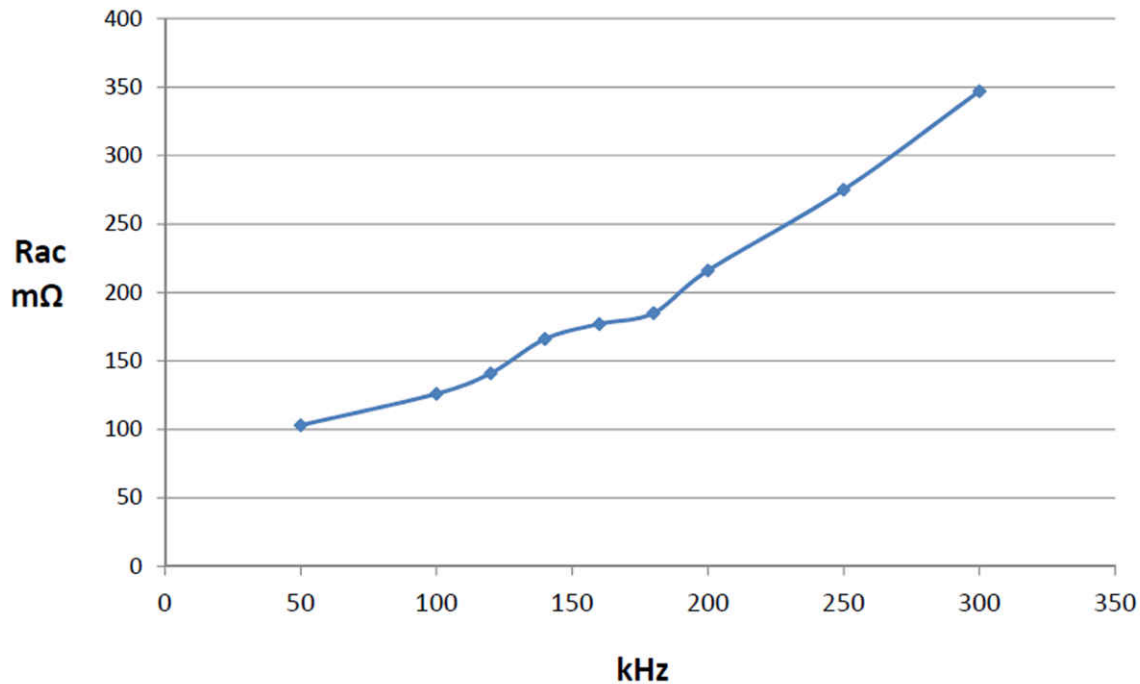
Figure 2-25. AC Resistance

$$P_{ac\_loss} = I_{prim\_rms}^2 R_{ac\_prim} + I_{sec\_rms}^2 R_{ac\_sec} = 10 \text{ W}$$

(32)

The core loss, copper losses, and skin effect losses together contribute 50 W of transformer loss. The 10-kW planar transformer designed with Payton is summarized in Table 2-2:

Table 2-2. Transformer Specifications

Functional specifications	Ratings
Total output power	10 kW (500 V/20 Adc)
Operating frequency	100-200 kHz
Input voltage of transformer	800 V (Vout = 500 V), Bipolar Square waveform;
Volt-second product	8000 V µs – for Vout = 500 V, 100 kHz;
Primary-to-secondary ratio	24:15
Primary current maximum	13.5 Arms (20 A peak) – for Vout = 500 V;
Secondary current maximum	20 Arms (30 A peak) – for Vout = 500 V;
Estimated power losses	50 W – for Vout = 500 V, 100 kHz;
Primary winding DC resistance	43 mΩ
Secondary winding DC resistance	16 mΩ
Leakage inductance	34 µH
Magnetizing inductance	720 µH

More details of this transformer are available from Payton.

2.3.5.4 Inductor Losses

The inductor used for this design is a custom inductor, which is integrated in the Payton planar transformer. The total leakage inductance is 34 µH and its total estimated power loss is about 15 W (for V_{OUT} = 500 V, 100 kHz).

2.3.5.5 Gate Driver Losses

The power loss in the gate driver circuit includes the losses in the UCC21530 and losses in the peripheral circuitry like the gate resistors. The power losses consist of the static power loss, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. Values of the static current flowing into the V_{cc1} pin (I_{vcc1}) , V_{DDA} pin (I_{DDA}) , and V_{DDB} pin (I_{DDB}) are extracted from the data sheet.

$$P_{static} = V_{Vcc1}I_{ICC1} + V_{DDA}I_{DDA} + V_{DDB}I_{DDB} = 70 \text{ mW} \tag{33}$$

By substituting the values from the data sheet in Equation 33, the result is P_{static} losses of the gate driver around 70 mW. The other component of gate driver loss is the switching operation loss.

$$P_{sw} = 2(V_{DD} - V_{ss})Q_G F_{SW} = 0.8 \text{ W} \tag{34}$$

By substituting the value of VDD = 15 V, VSS = –4 V, FSW = 100 kHz, QG = 211 nC in Equation 34, the switching loss comes to 0.8 W. The gate charge for C3M0016120K (primary side MOSFET) is extracted from data sheet. Similarly, for the secondary side, the switching losses are calculated to be approximately 0.33 W. Gate charge, QG, for the C3M0030090K MOSFET is 87 nC and is obtained from the data sheet. Also during turn on and turn off of the MOSFETs, losses occur in the gate resistors. The turn on and turn off gate resistors are 5.11 Ω and 1 Ω. These resistors are chosen to dampen out the oscillations at the gate. The gate driver IC can source 4 A and sink 6-A peak current during the switching process. Taking an average value of this current pulse over a switching cycle, the turn on and turn off losses occurring in the gate resistors is given by Equation 35.

$$P_{cond} = I_{on}^2 R_{on} + I_{off}^2 R_{off} = 0.5 \text{ W} \tag{35}$$

This value comes to 0.5 W across one switch. Thus, the total losses occurring in the four gate driver cards is 10 W.

2.3.5.6 Efficiency

Table 2-3 summarizes the loss numbers from the previous sections and computes the theoretical efficiency at 10 kW.

Table 2-3. Loss Analysis

TYPE OF LOSS	LOSS (Watts)
SiC conduction loss in primary and secondary side	112
SiC turn off switching loss	36
SiC non-ZVS turn on loss	24
Transformer loss	50
Gate driver loss + shunt resistor losses	12
Inductor loss	15
Efficiency	97.5%

2.3.5.7 Thermal Considerations

The loss estimations also allow the heat output of the design to be characterized. Any electrical loss in the system is converted to waste heat. Thermal simulations were performed using the physical layout of the design by exporting a step 3D from Altium, as well as the expected energy losses. An off-the-shelf heat sink from Wakefield-Vette (OMNI-UNI-18-75) was selected to simplify the design process and provide a starting reference point for understanding the thermal performance. This data should be used as a starting point for a thermal solution and not a fully validated solution. The system was simulated using a worse-than-calculated thermal output of 25 W per switching device. This meant that 200 W of total power dissipation across all of the switches and an additional 75 W across the capacitor, transformer, and leakage inductor. Figure 2-26 shows the thermal simulation results.
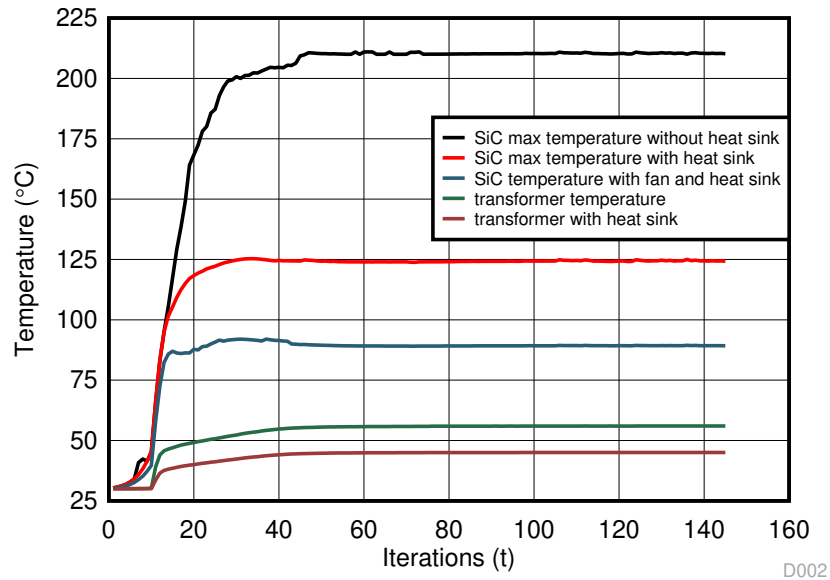
Figure 2-26. Simulated Temperature Versus Time

This simulation shows that the maximum junction temperature of the SiC MOSFETs, when run without heat sink close to the rated load of 10 kW, is approximately 210°C. When the heat sink is mounted to the FETs, the temperature rise is limited to 125°C. On using active airflow, the maximum temperature of the MOSFETs is contained to 90°C. Similarly, the transformer temperature is approximately 55°C without heat sink and around 45°C with heat sink.

In tests conducted at 10 kW, the maximum temperature recorded in the hard switching SiC MOSFET of the primary side was approximately 55°C, and the temperature on the secondary side SiC MOSFETs were approximately 35°C because of ZVS turn across all of them. The transformer temperature was approximately 40°C with heat sink. The measurements were taken using thermal imager under forced air cooling for the SiC MOSFETs alone.

3 Circuit Description

3.1 Power Stage

Figure 3-1 shows the power stage of a single-phase, dual-active bridge. The primary side consists of 1200-V, 16-mΩ silicon carbide FETs C3M0016120K(C3M0075120K can be an alternative part) to block a DC voltage of 800 V, and the secondary side consists of 900-V, 30-mΩ silicon carbide FETs C3M0030090K to block DC voltage of 500 V. The full bridges are connected with a high frequency switching transformer (T1). The components marked with DNP are not populated on the board. These are output capacitances for the MOSFETs, and they can be used optionally to reduce the turn off switching losses.
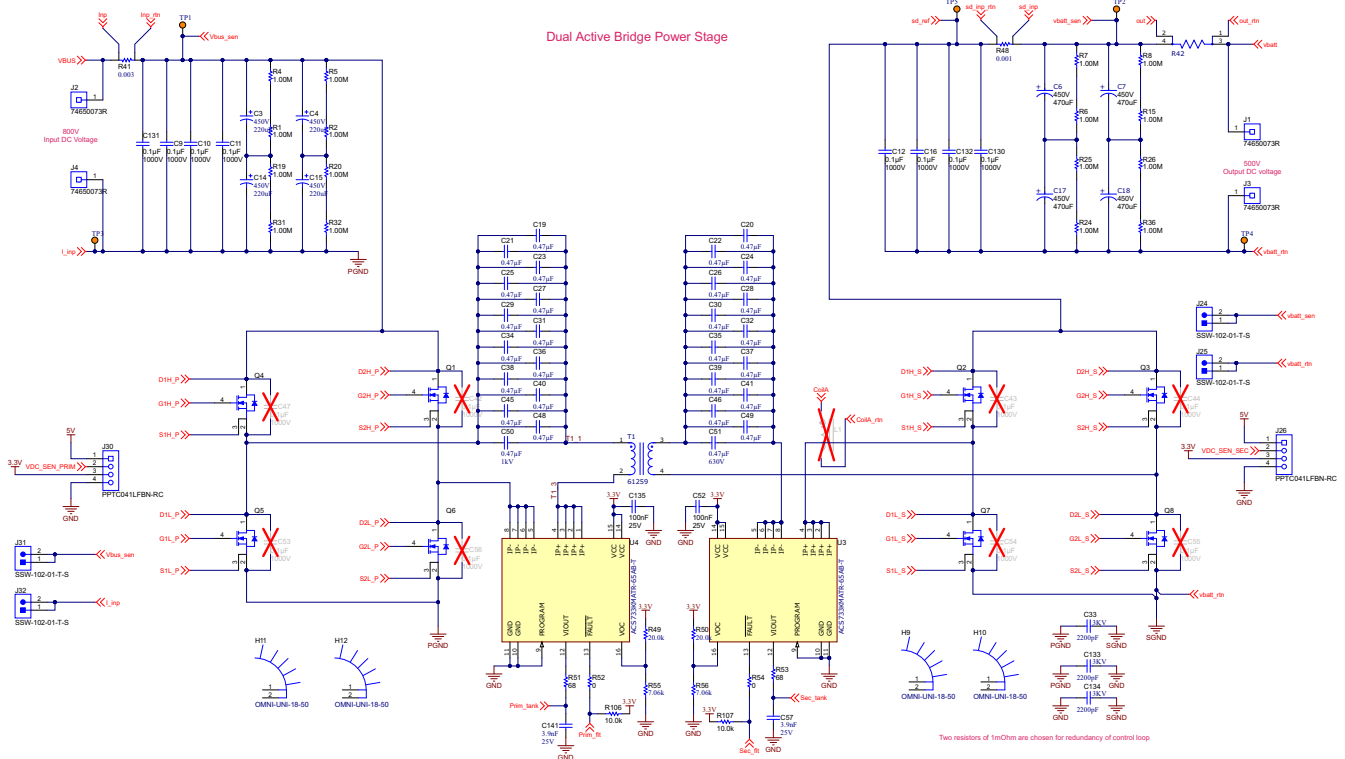
Figure 3-1. DAB Power Stage

3.2 DC Voltage Sensing

3.2.1 Primary DC Voltage Sensing

The design implements overvoltage protection by measuring the primary and secondary DC voltages. These voltages are scaled down using a resistive divider network and fed to the MCU using the AMC1311 reinforced isolation amplifier and the TLV9061. The output of the TLV9061 can directly drive the ADC input or can be further filtered before processed by the ADC.

Figure 3-2 shows the primary voltage sensing circuit. The maximum primary input voltage to be sensed is 800 V and is scaled down by a resistor divider network to 1.44 V, which is compatible to the 2-V input of the AMC1311. Figure 3-2 shows six 332-kΩ resistors and one 3.6-kΩ resistor used to drop the primary voltage signal. The signal is then processed by the TLV9061, which converts it in the range of 0 V to 3.3 V as required by the ADC.
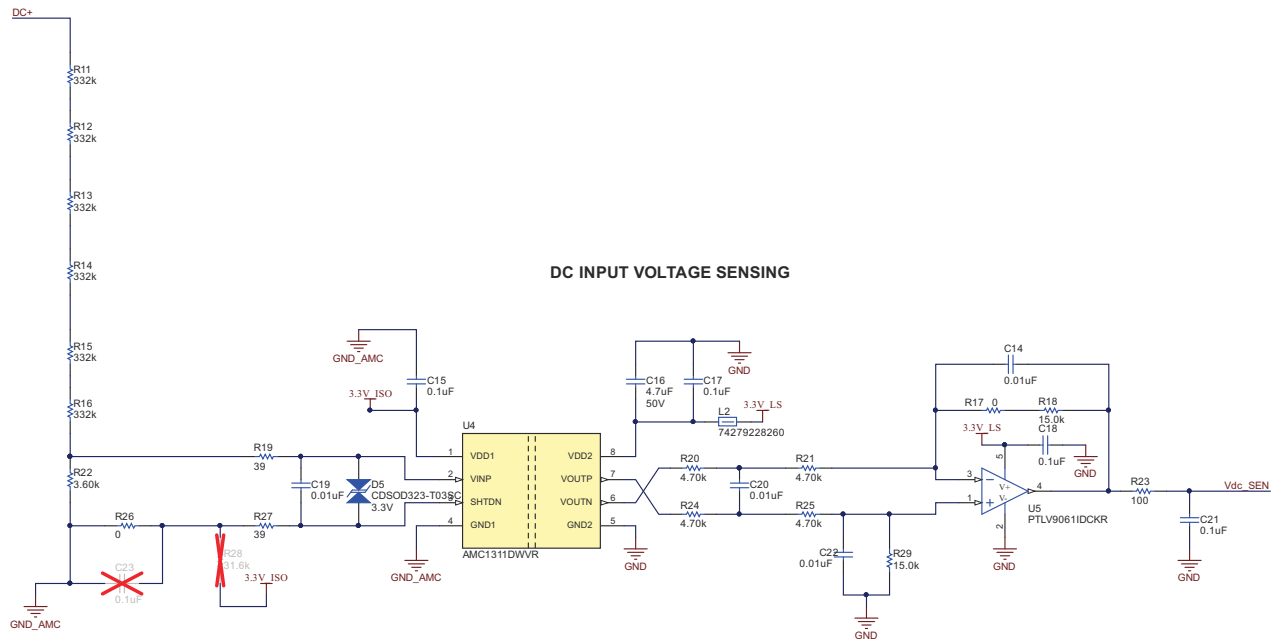
Figure 3-2. Primary Side DC Voltage Sense

[Figure 3-3](#) shows the isolated power supply circuit for powering the AMC1311. An isolated 3.3-V supply is needed to power the primary side of the AMC1311. This is accomplished through an SN6505 driving a push-pull transformer, which creates an isolated reference for the primary side. This isolated voltage is then regulated to 3.3 V using the TLV70433. The secondary side of the AMC1311 is powered with 3.3 V directly from the system power tree and is referenced to the controller GND.
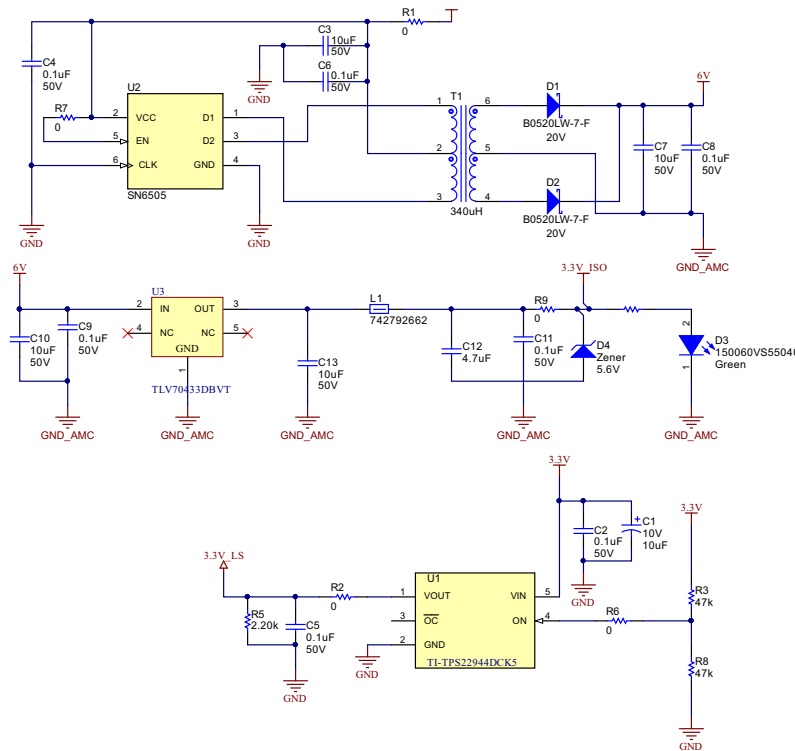
Figure 3-3. Isolated Power Supply for Primary

3.2.2 Secondary DC Voltage Sensing

Similar to the primary side voltage sensing, the maximum secondary input voltage to be sensed is 500 V and is scaled down by a resistor divider network to 1.44 V, which is compatible to the 2-V input of the AMC1311. Comparing with primary side voltage sensing circuit the only difference in secondary side is that the low side divider resistor is increased to from 3.6-kΩ to 6.5-kΩ.

3.3 Current Sensing

Current sensing is important for sensing overcurrent and getting a closed loop system to work accurately. In this design, current sensing is done at multiple locations with different sensing methods. The first is on the input and output side DC terminals using current sense resistors. The measured voltage across the sense resistor is given to the input of the AMC3302. The AMC3302 is a precision, isolated amplifier optimized for shunt-based current measurements. The fully integrated, isolated DC/DC converter allows single-supply operation from the low-side of the device, which makes the device a unique solution for space-constrained applications. The AMC3302, with a ±50-mV input and a fixed gain of 41, minimizes the power loss across the shunt. The positive and negative voltages are considered for bidirectional operation of the converter. A 1-mΩ and 2-mΩ four-pin shunt resistors with kelvin sense connections are used for accurate measurement of current. The ±50-mV input is scaled by a gain factor of 41 to produce ±2.05 V. This is then scaled and level shifted (by a 1.65-V reference) by the OPA320 to match the 0-3.3 V of ADC.

Sizing the shunt resistor for this design is a tradeoff between sensing accuracy and power dissipation. A 1-mΩ shunt at the input provides a voltage drop of ±12.5 mV at 12.5 Amp, and a 3-mΩ shunt at the output provides a voltage drop of ±49.5 mV at 16.5 Amp. Figure 3-4 and Figure 3-5 show isolated current sensing using the AMC3302.
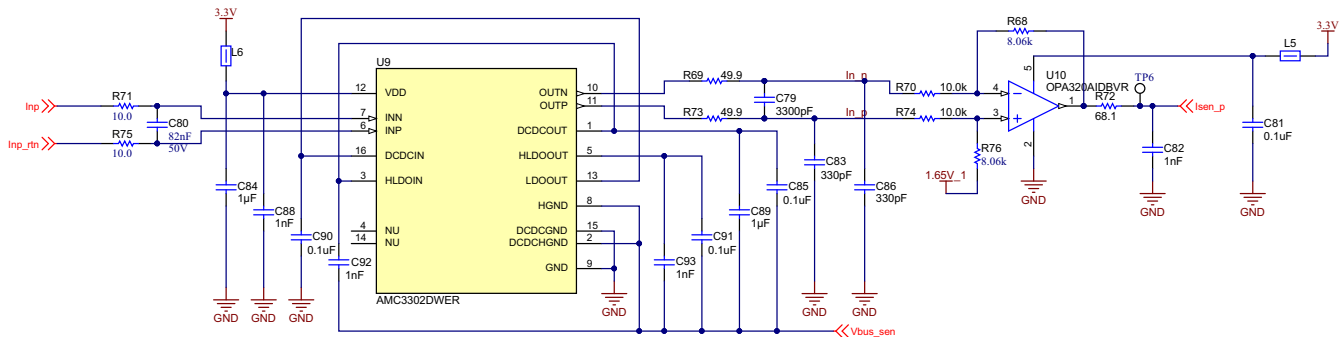
Figure 3-4. Isolated Sensing With AMC3302 in Primary
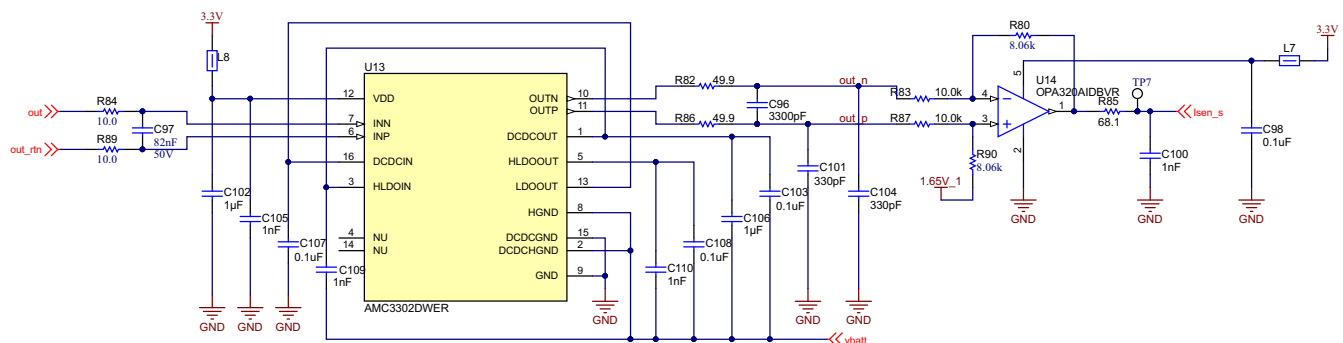
Figure 3-5. Isolated Sensing With AMC3302 in Secondary

To measure the switching currents across the secondary before the capacitor, the AMC3306M25 isolated reinforced modulator with a high bandwidth is used. The AMC3306M25 is a precision, isolated delta-sigma (ΔΣ) modulator, optimized for shunt-based current measurements. The fully integrated, isolated DC/DC converter allows single-supply operation from the low-side of the device, which makes the device a unique solution for space-constrained applications. The voltage across the shunt resistor is fed into the AMC3306M25 sigma-delta modulator, which generates the sigma-delta stream that is decoded by the SDFM demodulator present on the C2000™ MCU. Figure 3-6 shows isolated current sensing with the AMC3306. The clock for the modulator is generated from the ECAP/e-PWM peripheral on the C2000 MCU, and the AMC3306M25 data is decoded using the built-in SDFM modulator.
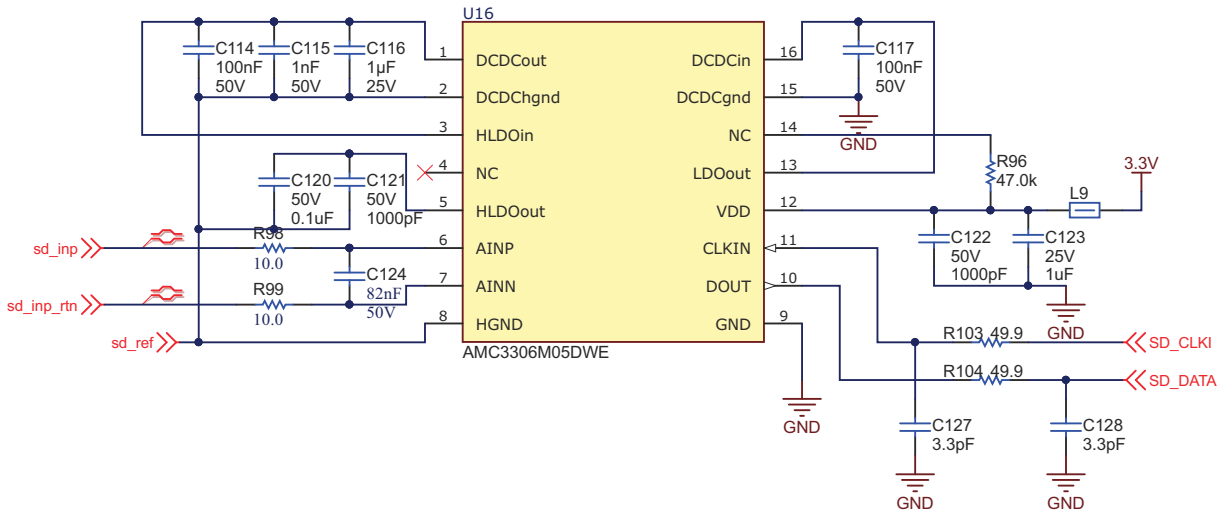
Figure 3-6. Isolated Current Sensing With AMC3306

There is a provision to measure primary and secondary tank current with hall sensor ACS733. The tank current can be used for overcurrent protection or detecting peak current of inductor.

3.4 Power Architecture

Figure 3-7 shows the system power tree used for multiple voltage domains across the system for powering discrete components.

- A primary voltage of 15 V (bench supply) to power up the auxiliary power tree components
- 12 V for cooling fan control
- 5 V and 3.3 V to drive the gate driver cards and DC bus HV sense cards
- On gate driver card isolated +15 V and –4 V are generated for biasing gate driver
- On HV sense card isolated +3.3 V is generated for biasing isolated amplifier
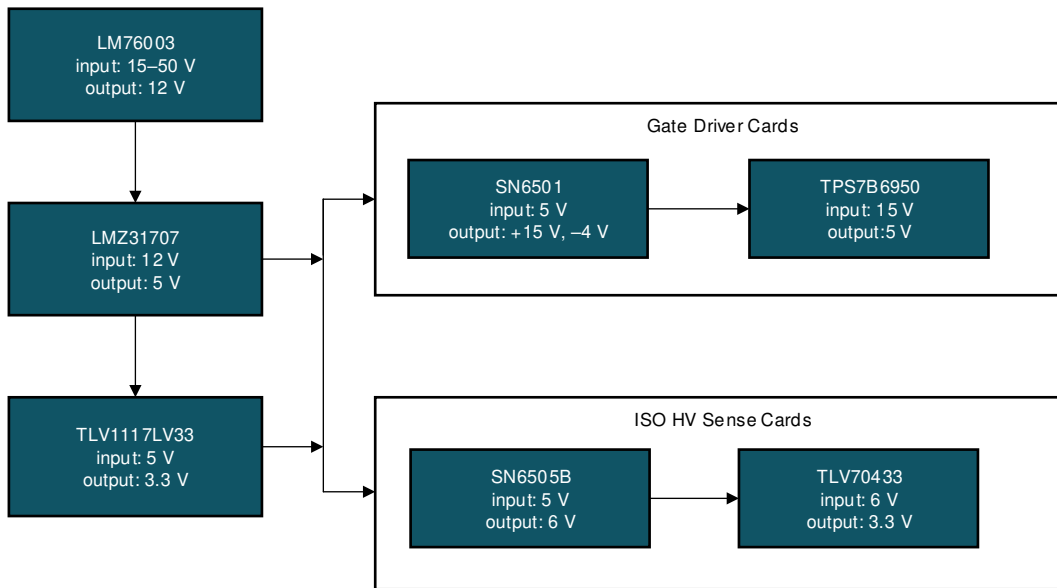
Figure 3-7. Power Architecture

3.4.1 Auxiliary Power Supply

The primary voltage for powering the auxiliary circuits is up to 50 V, which is given as input to the LM76003. The feedback resistors R59 and R60 are configured to provide an output voltage of 12 V. Figure 3-8 shows the LM76003 circuit.
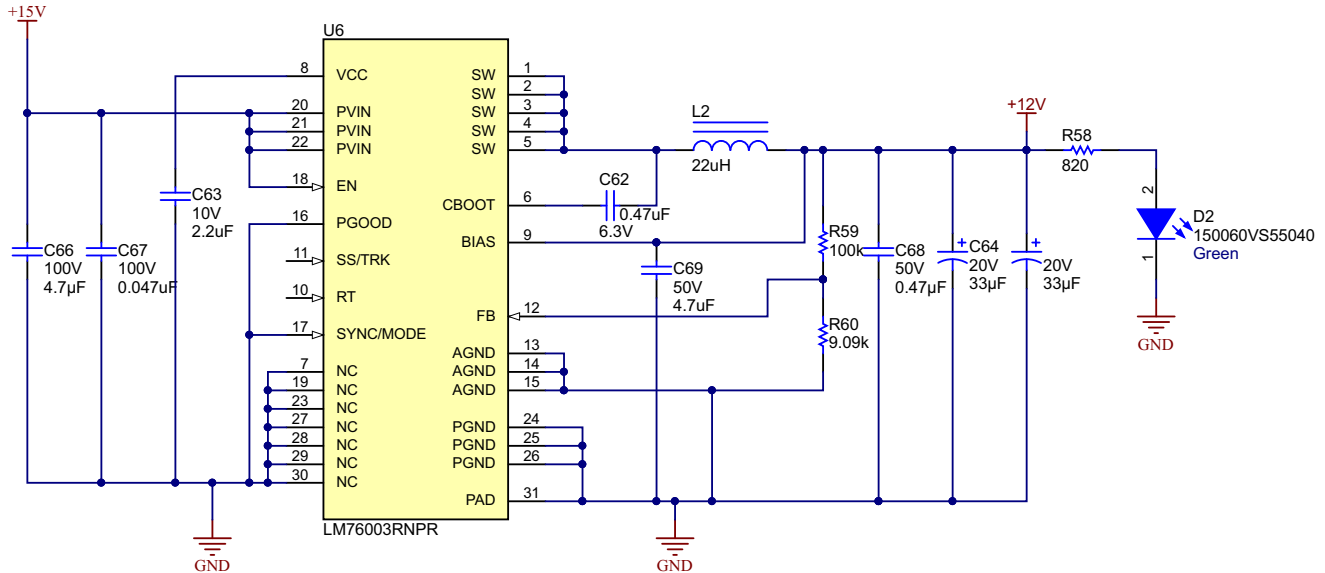
Figure 3-8. LM76003 Circuit

This 12-V rail is used to for cooling fan control and it is further scaled down to 5 V with LMZ31707. The LMZ31707 SIMPLE SWITCHER® power module is an easy-to-use integrated power solution that combines a 7-A DC/DC converter with power MOSFETs, a shielded inductor, and passives into a low profile, QFN package. Figure 3-9 shows the LMZ31707 circuit.
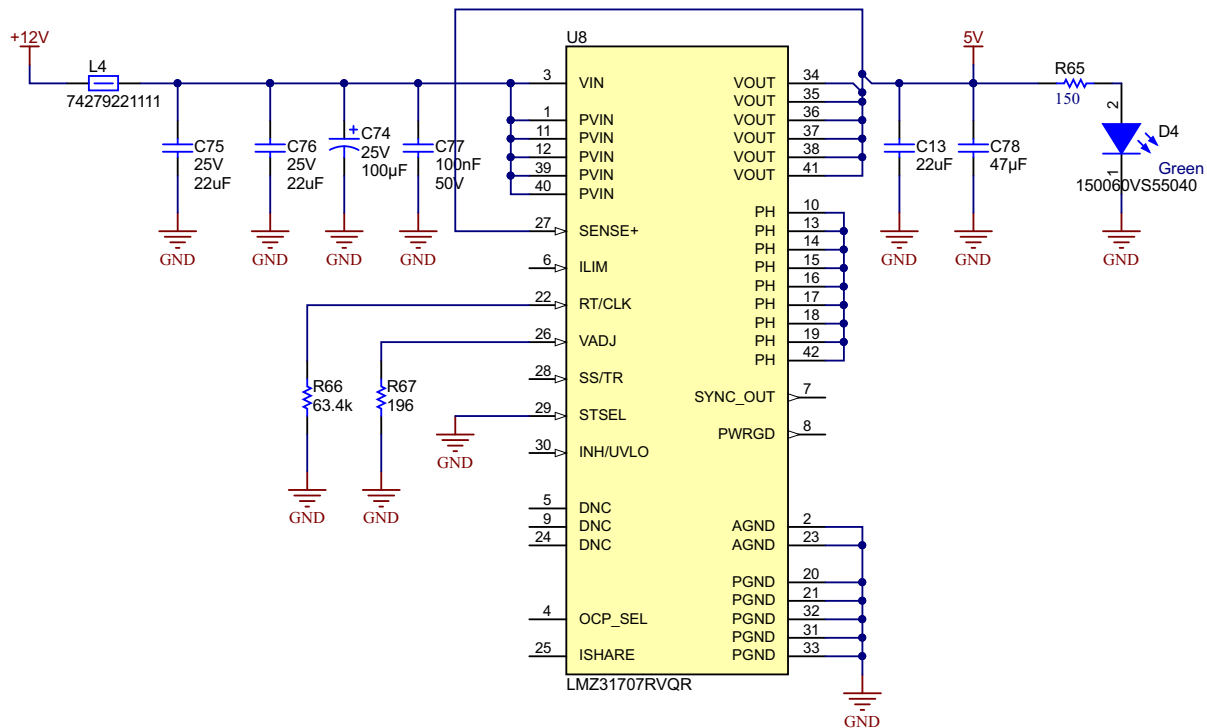
Figure 3-9. LMZ31707 Circuit

The other rail voltage of 3.3 V is produced by using the TLV1117LV33. The circuit is shown in Figure 3-10.
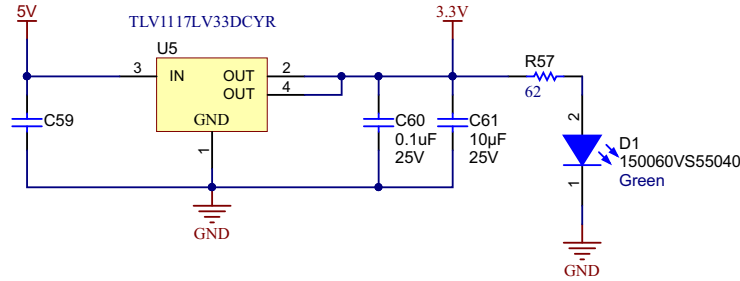
Figure 3-10. 3.3-V Circuit

3.4.2 Isolated Power Supply for Sense Circuits

To generate bias voltages for the AMC1311 isolated amplifiers, the SN6505B transformer driver is used to drive a Wurth 750313638 transformer in a push-pull configuration. The output of the push-pull stage produces a voltage of 6 V. The 6-V output is fed to a TLV70433 LDO to generate an isolated 3.3 V for driving the isolated amplifiers as shown in Figure 3-11.
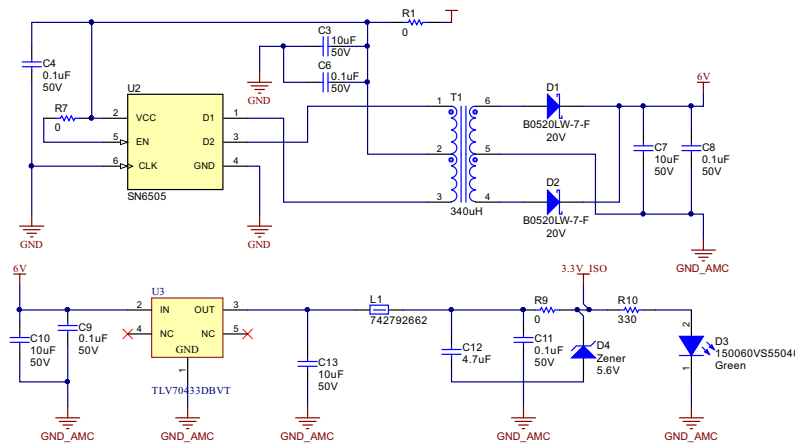
Figure 3-11. SN6505 Isolated Power Supply

3.5 Gate Driver

Figure 3-12 shows the block diagram of the gate driver daughter card inserted onto the main power board. The UCC21530 is the main gate driver driving the SiC MOSFETs of the power stage. Each block will be elaborated in detail in the following sections. For a detailed explanation on the selection of components and functionality of the UCC21530, see the Automotive Dual Channel SiC MOSFET Gate Driver Reference Design with Two Level Turn-off Protection.
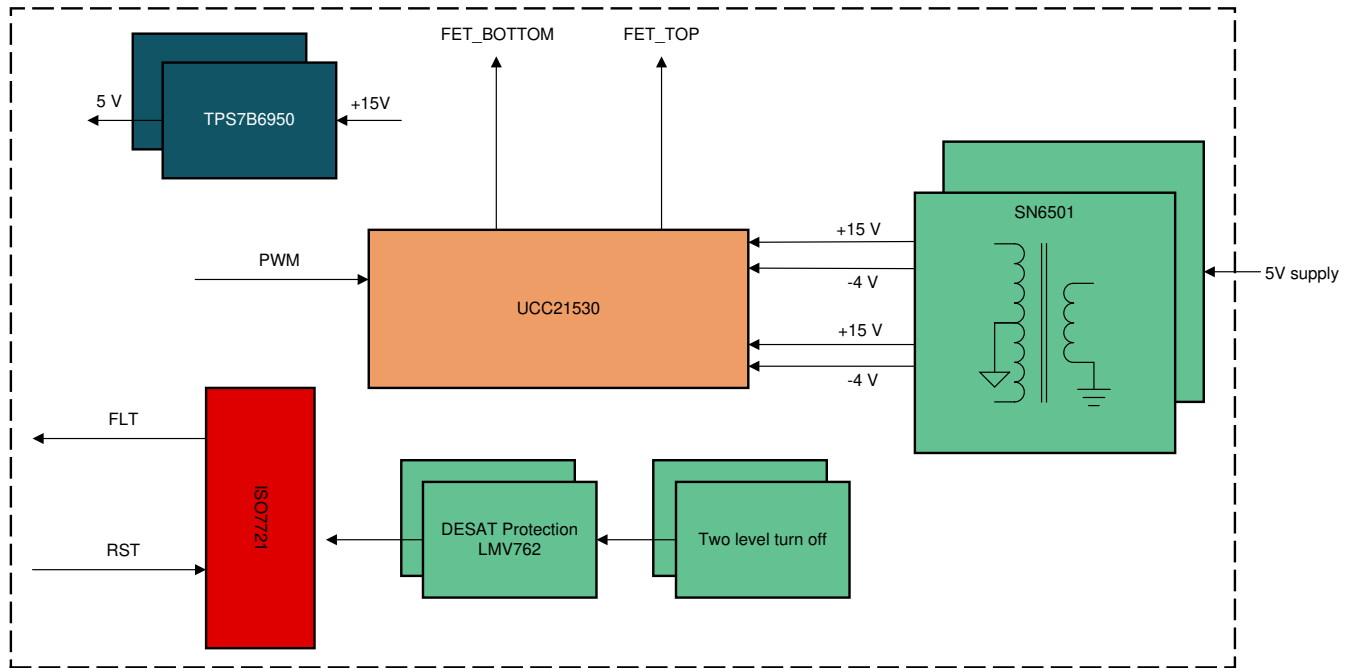
Figure 3-12. Gate Driver Card Block Diagram

3.5.1 Gate Driver Circuit

Figure 3-13 shows the schematic diagram of the isolated SiC MOSFET gate driver UCC21530. The UCC21530 device has 5.7-kV$_{RMS}$ isolation capability between the controller side and power side switch. The UCC21530 can be configured as either two low-side gate drivers or one single-half-bridge driver. The 3.3-mm, driver-to-driver spacing enables higher DC bus voltages.
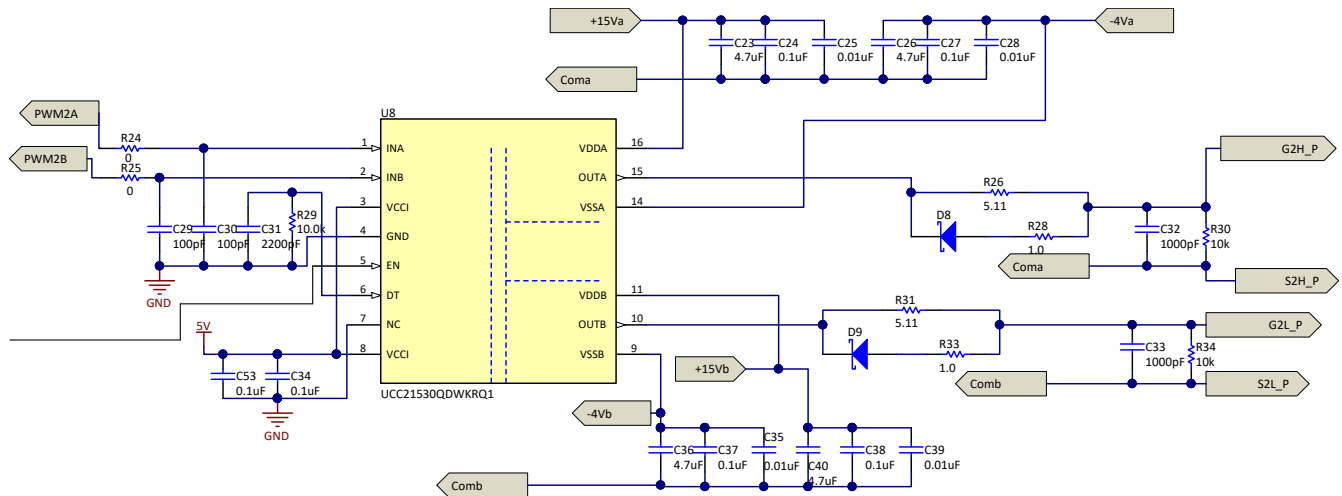
Figure 3-13. Gate Driver Circuit

The resistors R26 and R28 are the gate turn on and gate turn off resistors for the top SiC MOSFET, and R31 and R33 are the gate turn on and turn off resistors for the bottom SiC MOSFET. The PWM signals from the controller interface with pins INA and INB. There is also a hardware-configurable dead time provision available. The isolated bias voltages of 15 V and -4 V for driving the power stage of the gate driver is explained in the following section.

3.5.2 Gate Driver Bias Power Supply

Figure 3-14 shows the bias power supply voltage architecture, which enables to drive the gates across the isolation barrier. There are a total of 4 gate driver cards driving the primary and secondary side FETs. Each gate driver card consists of two bias voltage generators: one for driving the top-side FET and the other for driving the bottom-side FET. Overall, there are 8 bias supplies across the 4-gate driver boards used for this reference design. Figure 3-15 shows the implementation of the gate drive bias power supply.
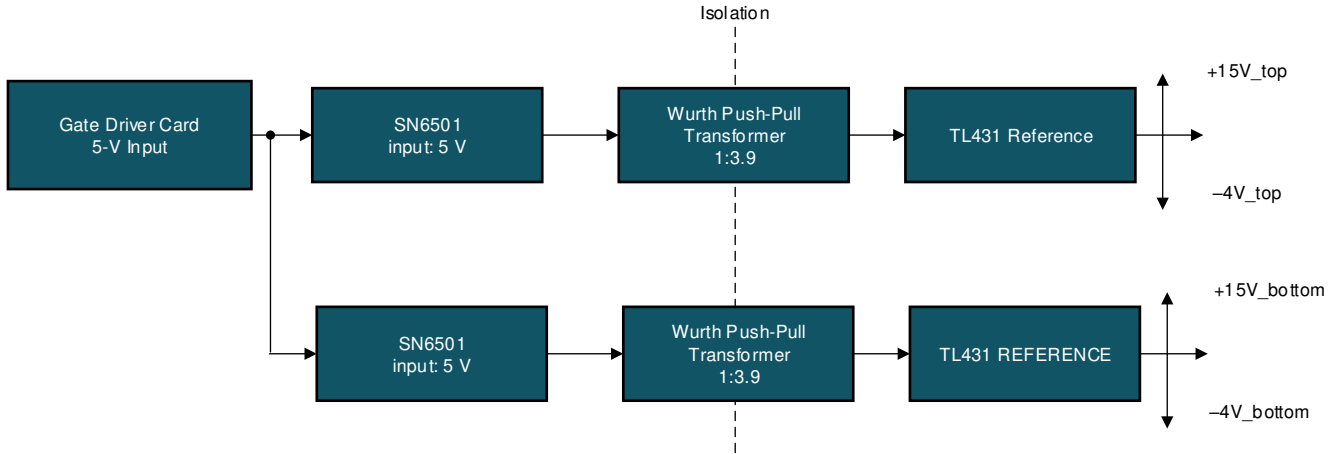
Figure 3-14. Gate Driver Bias Supply Architecture
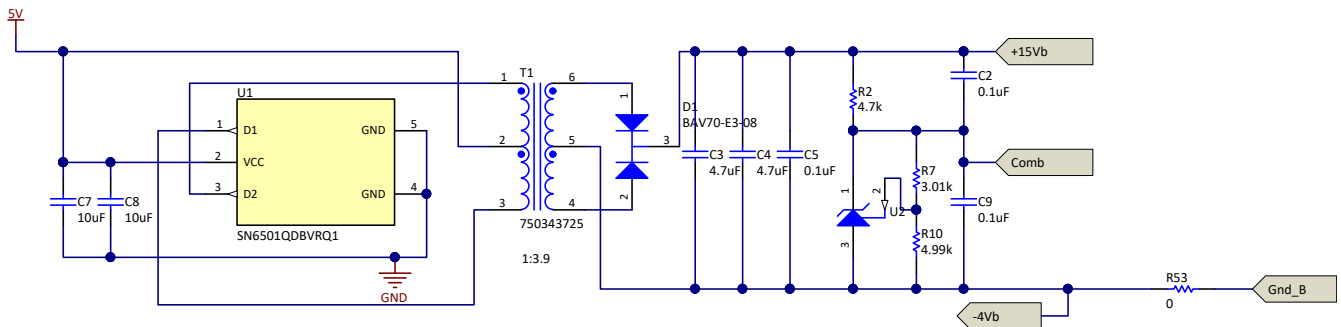
Figure 3-15. Gate Driver Bias Supply Circuit

The 5 V across the primary is translated to approximately 19 V in the secondary with a transformer turns ratio of 1:3.9. This is then separated into a positive rail of 15 V and negative rail of –4 V using the TL431 shunt regulator. The resistors R7 and R10 create a voltage reference of 4 V according to Equation 36.

$$V_{ref} = \left(1 + \frac{R_7}{R_{10}} \right) V_{shunt}$$

(36)

The shunt regulator reference voltage is 2.5 V.

3.5.3 Gate Driver Discrete Circuits - Short-Circuit Detection and Two Level Turn Off

SiC MOSFETs work in the linear region during normal operation. Unlike IGBTs, which have a sharp transition from saturation to active region, SiC MOSFETs have a large linear region and do not have a sharp saturation behavior under conditions with excessive currents. The transition to saturation region happens at significantly high drain source voltage (V_{ds}) and the drain current (I_d) reaches significantly high value, which can be as high as 15 times the normal current and can blow out the device. A DESAT detection circuit is necessary to detect this condition and protect the SiC MOSFET.

Figure 3-16 shows the circuitry for detecting short circuits. The diode, D6, interacts with the high-voltage drain pin of the MOSFET. At the start of the short circuit, the current flowing in the MOSFET channel increases dramatically until saturation, and the voltage from drain-to-source also increases and can reach up to the DC bus

voltage. The voltage built up across C14 is compared with a voltage reference (3 V) set by the shunt regulator TL431 using the LMV762, which triggers the protection stage to shut down gate driver IC. See the Automotive Dual Channel SiC MOSFET Gate Driver Reference Design with Two Level Turn-off Protection for details on working with this circuit.
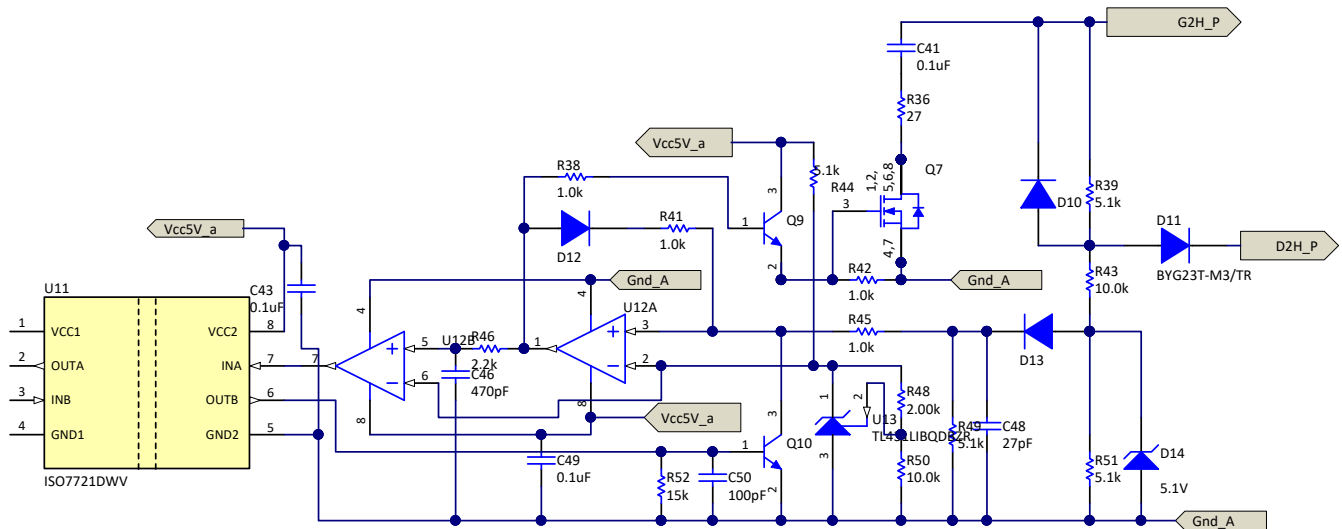
Figure 3-16. Short-Circuit Detection of SiC

In the event the SiC experiences a short circuit, it is detected and turned off. During the turn off process, the voltage overshoot can exceed the breakdown down voltage of the device and can destroy the switch completely. To avoid this, a two-level turn off process is initiated where the SiC MOSFET, instead of completely turning off in one shot, is made to turn off at two levels. This helps in preventing overshoot across the switch and keeps it within the safe operating area. Figure 3-16 shows the circuit for the two-level turn off process where a dual comparator, LMV762 (U4A and U4B), is used to initiate turn off by discharging the capacitors of the gate at two voltage levels. The capacitor C1 and R1 form an RC circuit which discharges the gate to a lower voltage level during turn off. The resistor R14 and C11 are used to set the delay time between the turn off transitions.

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Required Hardware and Software

4.1.1 Hardware

The hardware for this reference design is composed of the following boards:

- One TIDA-010054 power board
- Four TIDA-010054 gate driver cards
- Two TIDA-01606 ISOHV sense cards
- One TMDSCNCD280049C control card
- Mini USB cable
- Laptop

The following test equipment is needed to power and evaluate the DUT:

- 10-kW DC source capable of delivering voltage between 700 V–800 V at required current
- 10-kW resistive load bank
- Power analyzer
- Dual channel +15-V, 4-A auxiliary bench power supply
- Oscilloscope
- Isolated voltage probes and current probes

4.1.2 Software

Code Composer Studio™ 8.x with C2000 powerSUITE and digital power SDK are used in this design.

The general structure of the project follows C2000Ware-DigitalPower-SDK Structure. For this design, <solution> is "DAB". The solution name is also used as the module name for all the variables and defines used in the solution. Hence, all variables and function calls are prepended by the DAB name (for example, DAB_vSecSensed_pu). This naming convention lets the user combine different solutions while avoiding naming conflicts.

1. The "<solution>.c/h" are solution-specific and device-independent files that consist of the core algorithmic code.
2. The "<solution>_board.c/h" are board-specific and device-dependent. This file consists of device-specific drivers to run the solution. If the user wants to use a different modulation scheme or a different device, the user is required only to make changes to these files, besides changing the device support files in the project.
3. The "<solution>-main.c" file consists of the main framework of the project. This file consists of calls to the board and solution file that help in creating the system framework, along with the interrupt service routines (ISRs) and slow background tasks.
4. The "<solution>-settings.h" file is where all project-level settings are made like defining frequency, mapping PWM and ADC channels to signals on the control card. This is a device specific file and needs to change from device to device.

4.1.2.1 Getting Started With Software

1. Install *Code Composer Studio (CSS)*
2. Compiler version 18.1.3.LTS is required for the code to compile, download through the app center, if it is not installed
3. Download and install C2000WareDigitalPowerSDK
4. Open CCS, go to project → Import project and browse to the folder C:\c2000ware_digital_power_sdk\solutions\tida_010054\f28004x\ccs. The DAB project is listed. Complete the steps to import the project.
5. The code is designed for the F28004x control card. Figure 4-1 shows the loaded project explorer view. Open main.syscfg in project explorer window, choose lab and then compile, program the device.
6. Once loaded, enable real-time mode and run the code.
7. To add the variables in the watch or expressions window, click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on open and then browse to the "setupdebugenv_lab1.js" script file located inside the project folder. This populates the watch window with appropriate variables needed to debug the system.

8. Select the *Continuous Refresh* button on the watch window to enable continuous updates of values from the controller. Figure 4-13 illustrates the watch window.

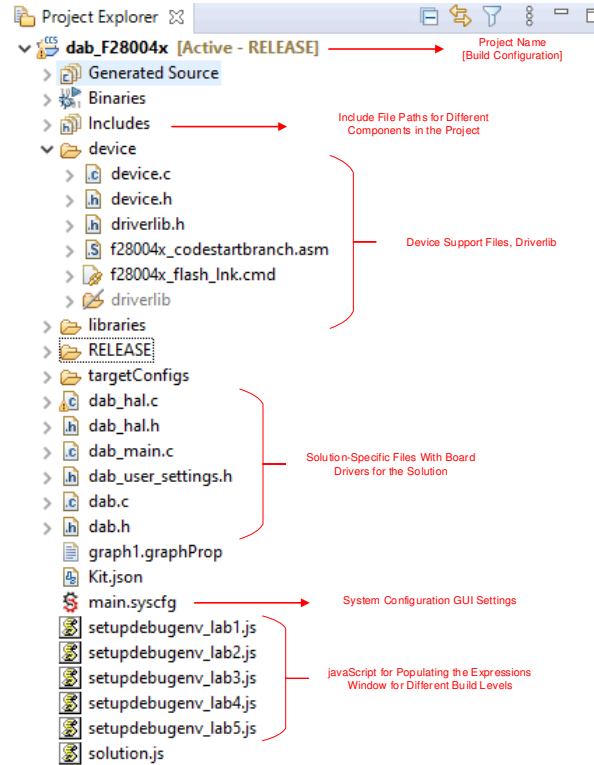**Figure 4-1. Project Explorer View**

4.1.2.2 Pin Configuration

Table 4-1 shows the key signal connections between the TMS320F280049C control card and TIDA-010054 base board.

Table 4-1. Key Peripherals for Control of the Power Stage on the Board

SIGNAL NAME	DESCRIPTION	CONNECTION TO ControlCARD (HSEC PIN)
PWM-1A	Primary side leg-1 high side drive	GPIO-00 (49)
PWM-1B	Primary side leg-1 low side drive	GPIO-01 (51)
PWM-2A	Primary side leg-2 high side drive	GPIO-02 (53)
PWM-2B	Primary side leg-2 high side drive	GPIO-03 (55)
PWM-3A	Secondary side leg-1 high side drive	GPIO-04 (50)
PWM-3B	Secondary side leg-1 low side drive	GPIO-05 (52)
PWM-4A	Secondary side leg-2 high side drive	GPIO-06 (54)
PWM-4B	Secondary side leg-2 high side drive	GPIO-07 (56)
Iinp_sense	Primary/Input DC current sense	ADC-C5 (31)
Ibatt_sense	Secondary/output current sense	ADC-B6 (15)
Vdc_sense_sec	Secondary/Output Voltage sense	ADC-B4 (24)
Vdc_sense_prim	Primary/Input Voltage sense	ADC-C0 (26)
Itank_SD_data	Sigma delta input from AMC3306	GPIO-27 (109)
Itank_clk	Clock signal for AMC3306	GPIO-24 (75)
Control Card UART	Reserved for control card UART	GPIO-28 (76)
Control Card UART	Reserved for control card UART	GPIO-29 (78)
Itank_prim_hall	Primary side tank current sensing with hall sensor	ADC-A6(25)

Table 4-1. Key Peripherals for Control of the Power Stage on the Board (continued)

SIGNAL NAME	DESCRIPTION	CONNECTION TO ControlCARD (HSEC PIN)
Itank_sec_hall	Secondary side tank current sensing with hall sensor	ADC-A9(27)

4.1.2.3 PWM Configuration

Up-down count mode is used to generate the PWMs for the primary and secondary legs of the dual active bridge. To use the high-resolution PWMs, the PRIM_LEG1_H PWM pulse is centered on the period event and the time base is configured to be up-down count. A complementary pulse with high-resolution dead time is then generated for the complementary switch. Between LEG1 and LEG2, there is a 180-degree phase shift for a full-bridge operation. This is achieved by using the feature on the PWM module to swap the xA and xB output. The PWM frequency for this application is 100 kHz. The TBPRD register is set to a value 500 in up-down count mode.

The duty cycle value is loaded in CMPA register of the EPWM base and is configured to generate 50% duty cycle. The action qualifier module outputs the required action for controlling the PWM output on a compare A event. The global link mechanism on the Type-4 PWM is used to reduce the number of cycles needed to update the registers and enables high-frequency operation. For example, the following code in the DAB_HAL_setupPWM() function links the TBPRD registers for all the PWM Legs.

Using this linkage, a single write to the PRIM_LEG1 TBPRD register writes the value to PRIM_LEG2, SEC_LEG1, and SEC_LEG2.

```
EPWM_setupEPWMLinks(DAB_PRIM_LEG2_PWM_BASE,EPWM_LINK_WITH_EPWM_1,EPWM_LINK_TBPRD);

EPWM_setupEPWMLinks(DAB_SEC_LEG1_PWM_BASE,EPWM_LINK_WITH_EPWM_1,EPWM_LINK_TBPRD);

EPWM_setupEPWMLinks(DAB_SEC_LEG2_PWM_BASE,EPWM_LINK_WITH_EPWM_1,EPWM_LINK_TBPRD);
```

Figure 4-2. PWM Write

4.1.2.4 High-Resolution Phase Shift Configuration

High-resolution features used:

- High-Resolution Phase Shift
- High-Resolution Dead Band
- High-Resolution Duty → Not available, CTMODEB is set to 1
- High-Resolution Period → Not available, CTMODEB is set to 1

The PWM pulses of the secondary side are phase-shifted with respect to the PWM pulses of the primary. Controlling the phase shift enables transfer of power between the primary and secondary and vice versa. The maximum power transferred is very sensitive to the value of phase shift in a Dual Active Bridge. A small series inductor can lead to maximum power transfer at a small value of phase shift. Since the range over which the phase shift is going to be varied is small, and accurate control would require fine increment and decrement steps of phase. The phase control is implemented using Hi-Res (high resolution) feature of F28004x. The function DAB_calculatePWMDutyPeriodPhaseShiftTicks() inside ISR1 calculates the required the required high resolution phase control for both voltage and current mode control. This helps in handling sudden load changes smoothly without producing huge overshoots/transients in the current waveforms.

```
static inline void DAB_calculatePWMDutyPeriodPhaseShiftTicks(void)
{
...
    //
    // first the phase shift in pu is converter to ns
    // this is done for better debug and user friendliness
    //
    DAB_pwmPhaseShiftPrimSec_ns = DAB_pwmPhaseShiftPrimSec_pu *
            ((float32_t)1.0 / DAB_pwmFrequency_Hz) *
            (1 / ONE_NANO_SEC);


    //
    // next this ns is simply converted to ticks
    //
    DAB_pwmPhaseShiftPrimSec_ticks =
            (int32_t)((float32_t)DAB_pwmPhaseShiftPrimSec_ns *
                    DAB_PWMSYSCLOCK_FREQ_HZ * ONE_NANO_SEC *
                    TWO_RAISED_TO_THE_POWER_SIXTEEN) -
            ((int32_t)2 << 16);


    //
    // due to the delay line implementation depending on whether it is
    // a phase delay or an advance we need to adjust the
    // HR phase shift ticks calculations
    //
    if(DAB_pwmPhaseShiftPrimSec_ticks >= 0)
    {
        DAB_phaseSyncPrimToSecCountDirection = EPWM_COUNT_MODE_DOWN_AFTER_SYNC;


        //
        // DAB_pwmPhaseShiftPrimSec_ticks has the correct value already
        //
    }
    else
    {
        DAB_phaseSyncPrimToSecCountDirection =  EPWM_COUNT_MODE_UP_AFTER_SYNC;
        DAB_pwmPhaseShiftPrimSec_ticks = DAB_pwmPhaseShiftPrimSec_ticks * -1;

        DAB_pwmPhaseShiftPrimSec_HiResticks =  ((uint16_t) 0xFF - ((uint16_t)
                (DAB_pwmPhaseShiftPrimSec_ticks & 0x0000FFFF)>>8));

        DAB_pwmPhaseShiftPrimSec_ticks = ((DAB_pwmPhaseShiftPrimSec_ticks & 0xFFFF0000) + 0x10000) +
                (DAB_pwmPhaseShiftPrimSec_HiResticks << 8);
    }
}
```

Figure 4-3. PWM Function 1

```
static inline void DAB_HAL_updatePWMDutyPeriodPhaseShift(uint32_t period_ticks,
                                  uint32_t dutyAPrim_ticks,
                                  uint32_t dutyASec_ticks,
                                  uint32_t phaseShiftPrimSec_ticks,
                                  uint16_t phaseShiftPrimSec_direction)
{
...
    EALLOW;
    HWREG(DAB_SEC_LEG1_PWM_BASE + HRPWM_O_TBPHS) = phaseShiftPrimSec_ticks;
    HWREG(DAB_SEC_LEG2_PWM_BASE + HRPWM_O_TBPHS) = phaseShiftPrimSec_ticks;
    EDIS;
}
```

Figure 4-4. PWM Function 2

The variable 'DAB_phaseSyncPrimToSecCountDirection' is updated to control the forward mode or reverse mode of power flow.
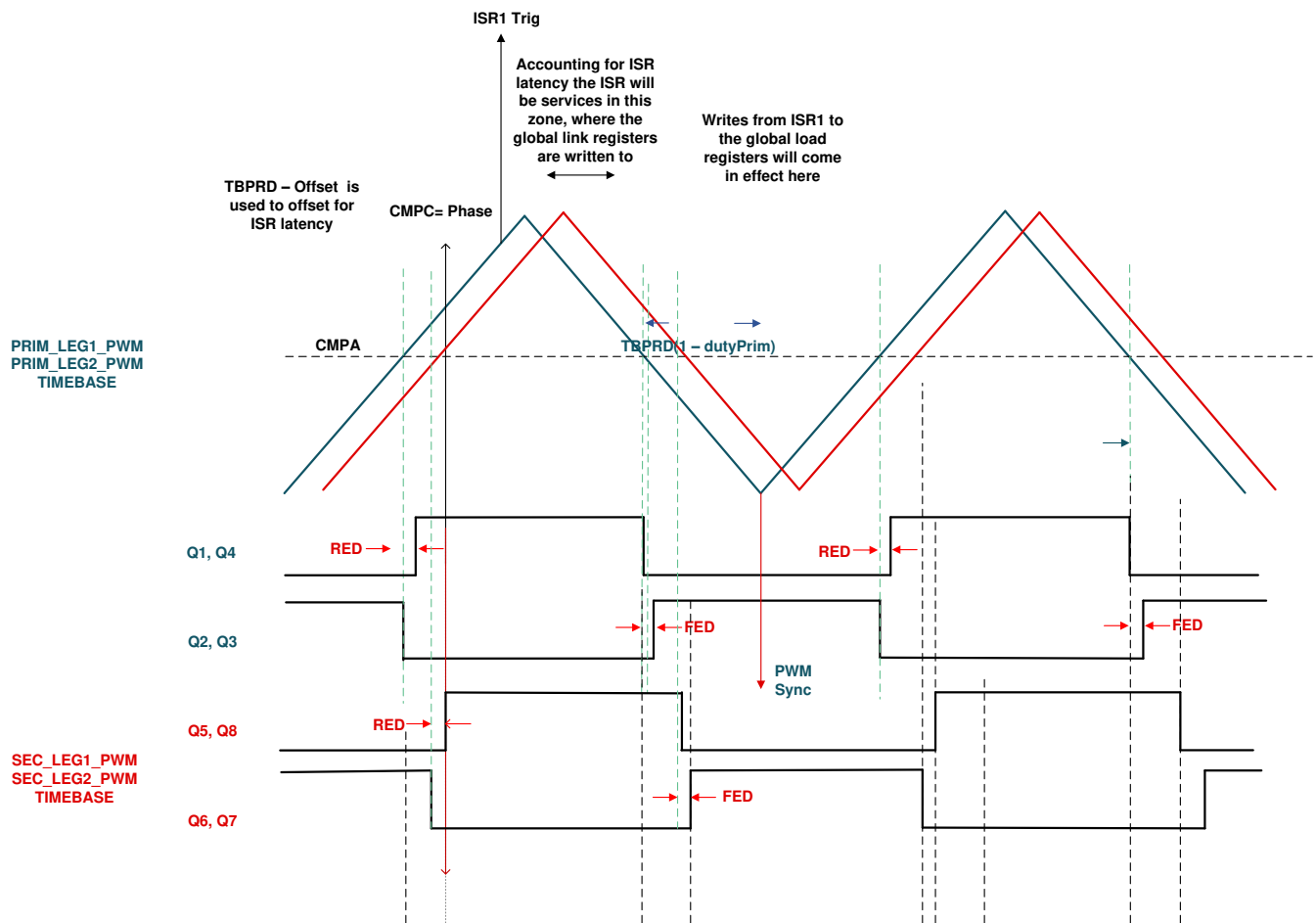
Figure 4-5. PWM Config

4.1.2.5 ADC Configuration

The configuration for ADC is done in the dab_main.c using the function DAB_HAL_setupADC(). The reference voltage, prescaling the clock and setting up SOC (start of conversions) for the voltage and current signals are done here. The trigger for ADC is generated from a start of conversion (SOC) signal from EPWM1. This configuration is done inside the function DAB_HAL_setupTrigForADC() in the dab_main.c file. All other settings mapping the HSEC card pin connector signals to the control card are done in the dab_settings.h file.

4.1.2.6 ISR Structure

The DAB project consists of two ISRs (ISR1 and ISR2) with ISR1 being the fastest and non-nestable ISR. ISR1 is reserved for the control loop and the PWM update. ISR1 is triggered by the PRIM_LEG1_PWM_BASE → EPWM_INT_TBCTR_U_CMPC event.

The following are the defines related to this ISR:

```
#define DAB_ISR1_PERIPHERAL_TRIG_BASE DAB_PRIM_LEG1_PWM_BASE
#define DAB_ISR1_TRIG INT_EPWM1
#define DAB_ISR1_PIE_GROUP INTERRUPT_ACK_GROUP3
#define DAB_ISR1_TRIG_CLA CLA_TRIGGER_EPWM1INT
```

ISR2 is triggered by CPU Timer INT which is initiated by an overflow on CPU timer. ISR2 runs the slew rate function for commanded references.

```
#define DAB_ISR2_TIMEBASE CLLLC_TASKC_CPUTIMER_BASE
#define DAB_ISR2_TRIG INT_TINT2
```

Additionally, CPU timers are used to trigger slow background tasks (these are not interrupt-driven but polled). "A" tasks are triggered at TASKA_FREQ, which is 100 Hz. The SFRA GUI must be called at this rate. One task, A1, is executed at this rate. "B" tasks are triggered at TASKB_FREQ, which is 10 Hz. These are used for some basic LED toggles and state machine items that are not timing-critical. Three tasks—B1, B2, and B3—are serviced by this.

Figure 4-6 illustrates the ISR software diagram.

Note

The EMAVG_RUN function is not used in the current software.
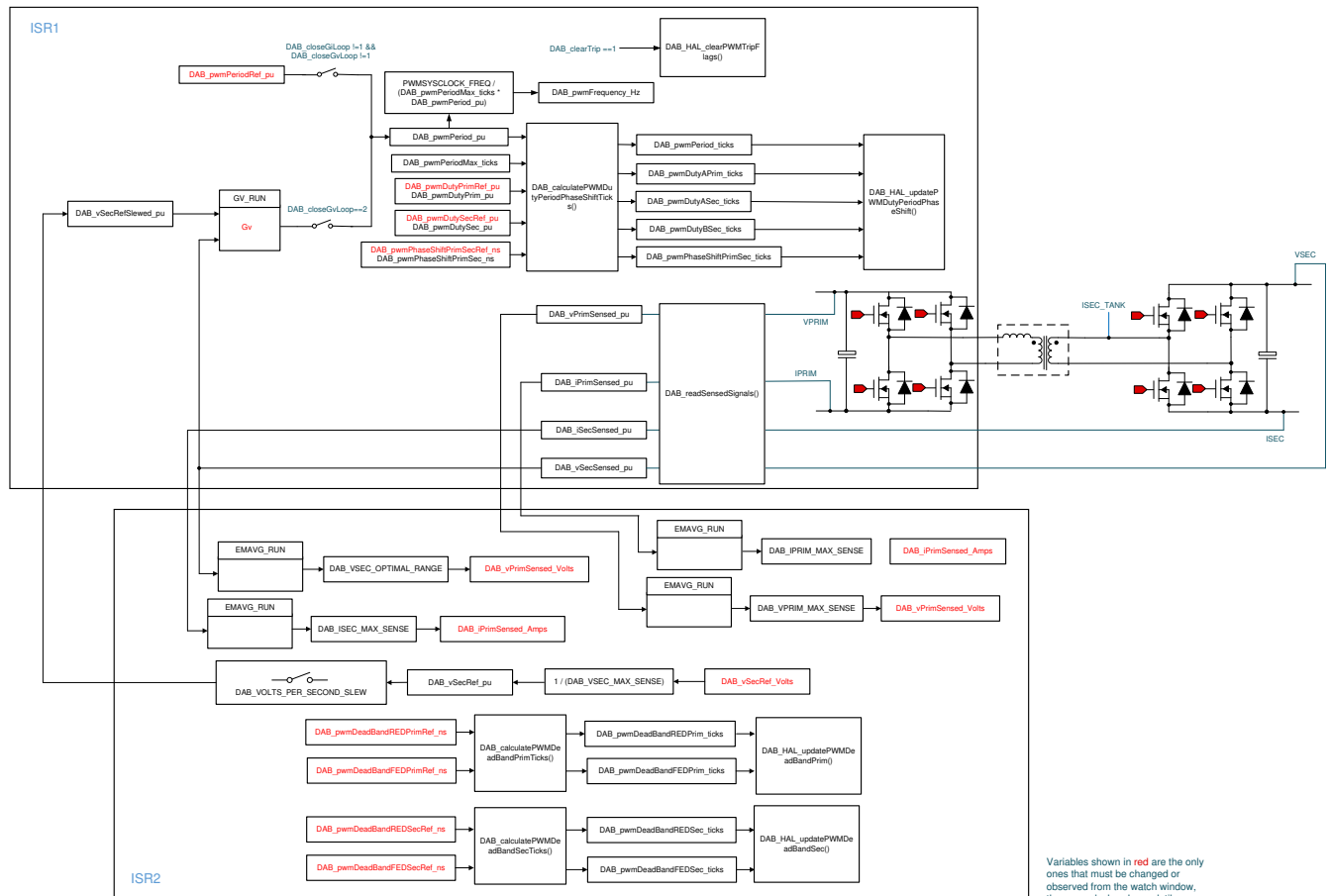
Figure 4-6. Software Diagram

4.2 Test Setup

To test the efficiency of this reference design, use the set up shown in Figure 4-7.

- Keysight® N8900 DC power supply
- Vitrek PA-900 power quality analyzer
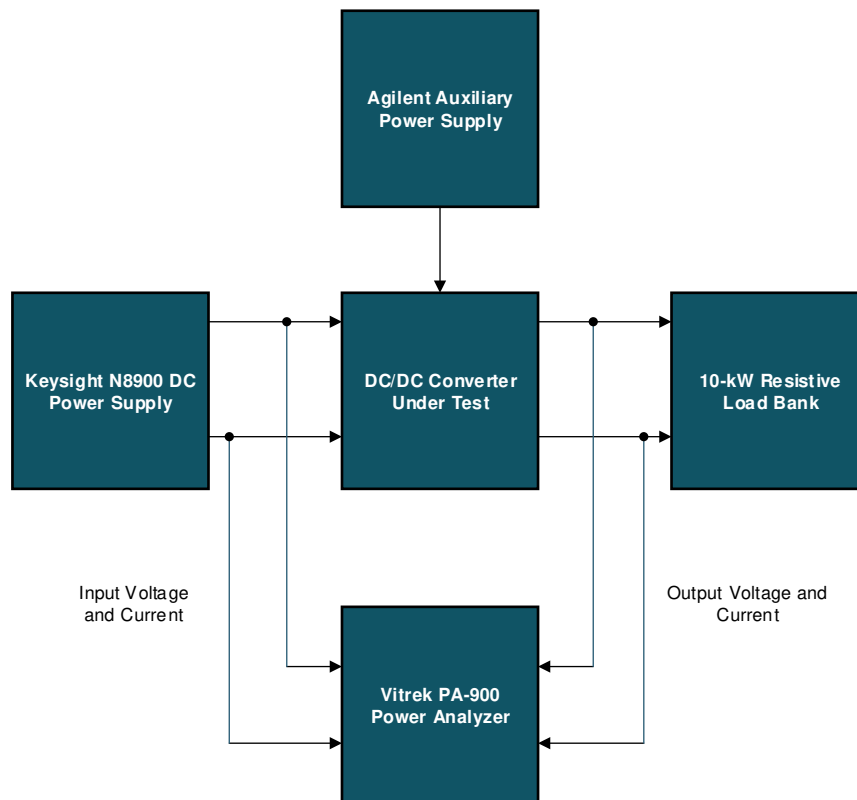
Figure 4-7. Test Setup
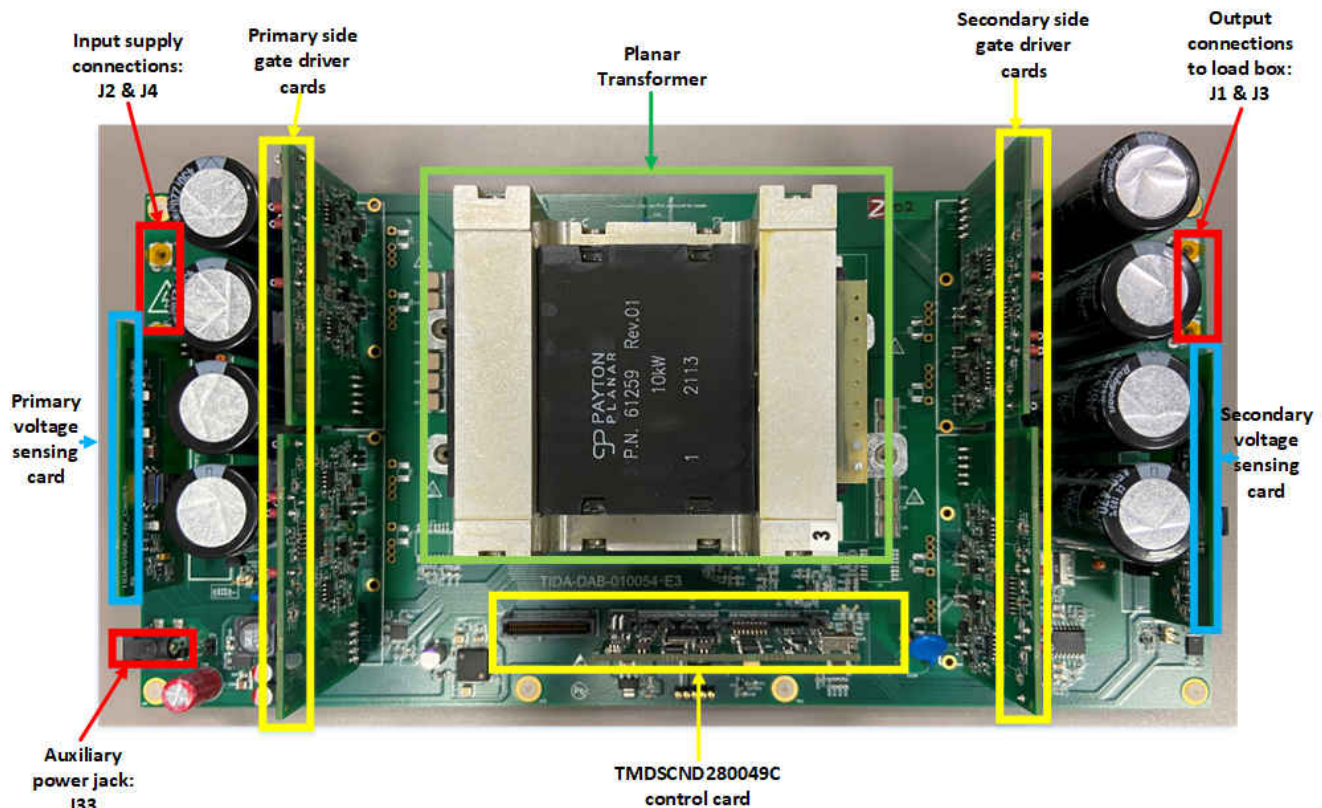
Figure 4-8. Board Image

Before powering the board to perform open-loop testing, use the following steps to set up the board:

1. Insert the four TIDA-010054 gate driver boards, HV sense boards and the control card carefully into their respective slots
2. Connect the terminals J2 and J4 to the input power supply and terminals J1 and J3 to the output load bank. Use a 4-mm^2 wire to make these connections so that they can handle high currents without getting heated quickly.
3. Connect the auxiliary power supply to terminal J33 using a PJ-002 female connector to power the controller, gate driver, and sense circuits

There is a cut-out area provided at the center of the board to mount the transformer. The transformer is directly connected to the board using M3 screws. Take care while mounting the transformer so that the primary and secondary sides are not interchanged.

The control card is programmed using a USB connection from the laptop to generate PWM pulses at 100 kHz. Once programmed, the auxiliary power supply is set to 15 V. No voltage should be applied across terminals J2 and J4. When the auxiliary power supply is turned on, it should take current of approximately 550 mA.

Once the auxiliary power supply is verified, voltage is applied across terminals J2 and J4. Initially, start with a voltage of 100 V and then slowly increase the voltage in steps of 50 V until 800 V is reached. See Section 4.5 for the required values of phase shift to be applied for a particular load condition.

Forced air cooling using SAN ACE 40GA20 were used to remove heat from MOSFET heat sink. Capacitors C42, C43, C44, C47, C53, C54, C55, and C56 are not populated on the board. These are placeholders for adding external snubber capacitors to help to reduce turn off losses. The current design does not have these capacitors populated on board.

Note

With the current hardware, the following changes are necessary to run the lab experiments:

1. Remove the resistor R13 and short pin 13 to pin 14 on device U1
2. Remove the resistor R30 and short pin 13 to pin 14 on device U2
3. Replace capacitors C57 and C141 with lower value capacitors between 2.2 nF and 4.7 nF to increase the bandwidth
4. Add a 330-pF parallel capacitor on R68 and R80 to reduce the noise
5. Change R22 to 6.5 kΩ on the HV sense card for secondary DC voltage sensing
6. The short-circuit detection and two-level turn-off function on the gate driver card is not currently supported . To avoid false alarms, unpopulate ISO7721.
7. The close loop bandwidth was tested with 220-µF DC link capacitors on the secondary side

Table 4-2. Connection Details

CONNECTOR TERMINALS	FUNCTION	COMMENTS
J2–J4	Input high voltage power supply	800-V DC power supply capable of sourcing 10-kW power
J1–J3	Output load terminals	10-kW resistive load bank is connected here
J33	Auxiliary power supply for gate driver, control card and sense circuits	15-V DC power supply current limited to 700 mA
J5	TMDSCNCD280049C Control card	Insert the control card here
J20, J23, J29, J18	Primary side gate driver card (Leg 1)	Insert the 4 gate driver cards here
J19, J22, J15, J27	Primary side gate driver card (Leg 2)	
J12, J13, J10, J11	Secondary side gate driver card (Leg 1)	
J16, J21, J28, J17	Secondary side gate driver card (Leg 2)	
J30, J31, J32	Primary side DC voltage sensing	Insert the 2 isolated DC HV sensing cards here
J24, J25, J26	Secondary side DC voltage sensing	

4.3 PowerSUITE GUI

PowerSUITE GUI was designed in this project for quick configuration of testing specifications. Figure 4-9 provides a detailed description of the PowerSUITE GUI. Open main.syscfg to configure the parameters for running various lab exercises.

Figure 4-9. PowerSUITE GUI Description

4.4 LABs

The software of this reference design is organized in five labs. These tests simplify the system bringup and design.

Table 4-3. Summary of Labs

LAB		WHAT IS THE LAB CHECKING?	COMMENTS
1	PWM Check, Power Flow Prim→ Sec	Verify power transfer from primary to secondary. Check PWM frequencies and also if Phase shift is working	
2	PWM Check, ADC check, Protection Check	Measure open loop plant for voltage and current. Check the feedback from Voltage and Current sensors. Ensure PWM signals are disabled while protection is enabled and trip flags are set.	Check the variable 'DAB_clearTrip'
3	Closed Voltage Loop - Vsec	Run the voltage mode compensator. Obtain open-loop transfer function of plant from SFRA. Design compensator for the plant In compensator design tool.	DF22 compensator implemented. Feedback variable is DAB_vSecSensed_pu
4	Closed current loop → Isec	Run the current mode compensator. Obtain open-loop transfer function of plant from SFRA. Design compensator for the plant In compensator design tool.	PI compensator implemented. Feedback variable is DAB_iSecSensed_pu
5	Reverse power flow Sec→ Prim	Verify power transfer from secondary to primary. Check PWM frequencies and also if Phase shift is working	

4.4.1 Lab 1

Compile the project by selecting *Lab 1: Open Loop PWM* in the drop-down menu of Project Options from PowerSUITE GUI. This lab is intended to validate the PWM outputs and can be checked directly using TIDA-010054 HW or using the F2804X control card with a docking station.

Run the project by clicking the green run button in CCS.
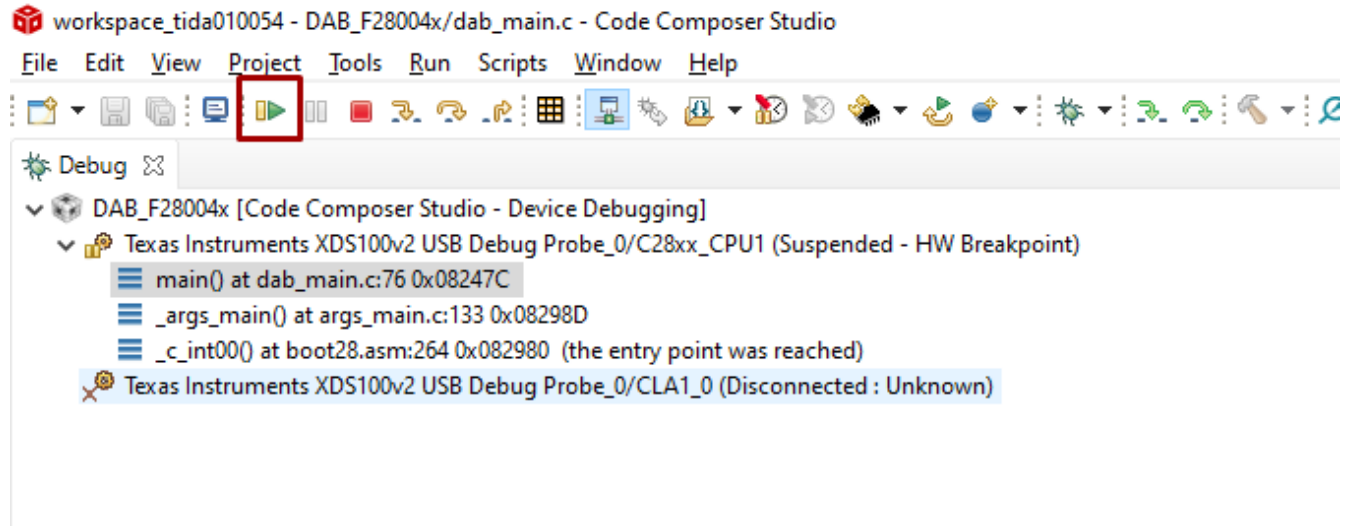
Figure 4-10. Run CCS

Populate the required variables in the watch window by loading javascript ' setupdebugenv_lab1.js' in the scripting console.

Figure 4-11. Loading Labs
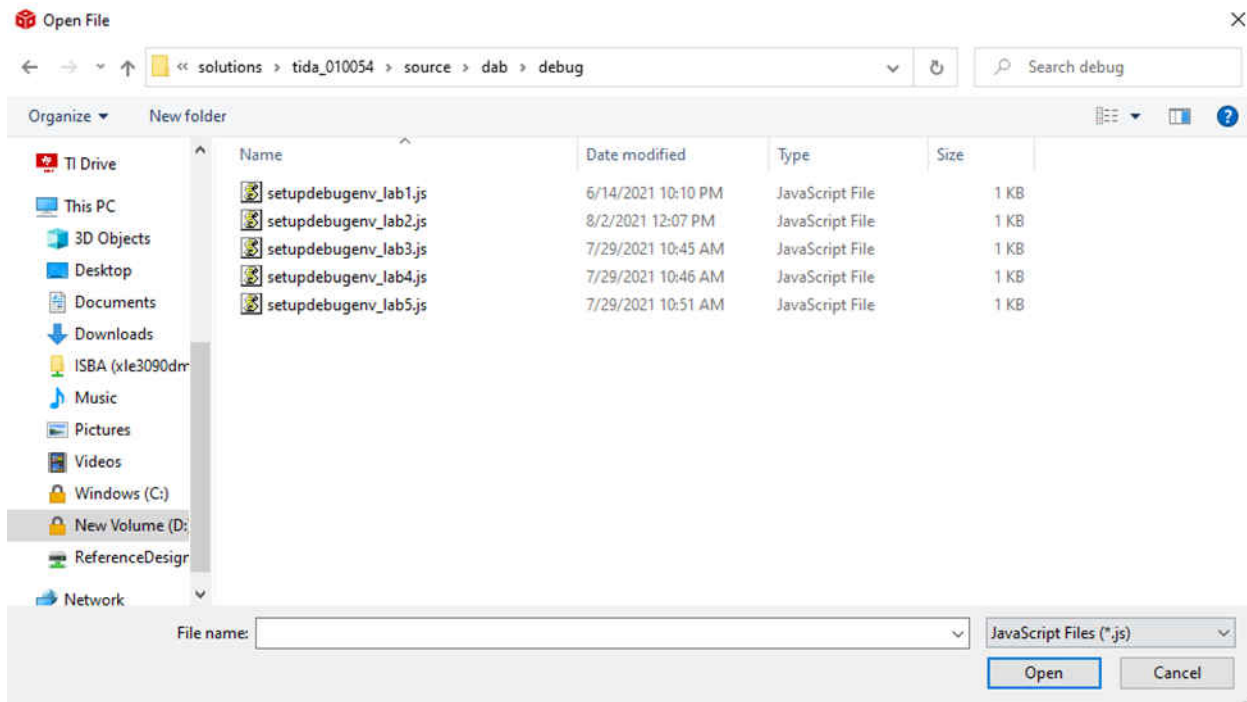
Figure 4-12. Select a Lab

1. After running the script, the watch window is populated with the variables in Figure 4-13.
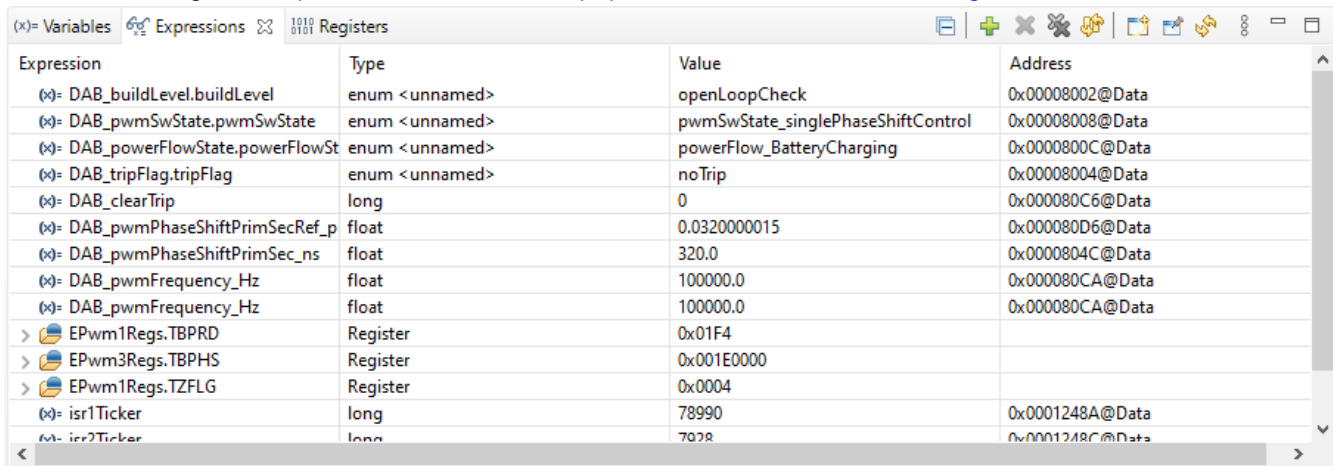
Figure 4-13. Watch Window

2. Enable PWM by writing "1" to the DAB_clearTrip variable. (This variable resets to zero post writing and its normal)

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- **Pass criteria for Lab1**

   Connect probes on PWM1A (Q1), PWM1B (Q2), PWM3A(Q5), and PWM3B (Q6).

   1A and 1B are a complimentary pair, 3A is in sync with 1A with the specified phase shift, and the phase shift is controlled by the variable, DAB_pwmPhaseShiftPrimSecRef_pu.

   Check the following:

   1. Frequency is 100 kHz
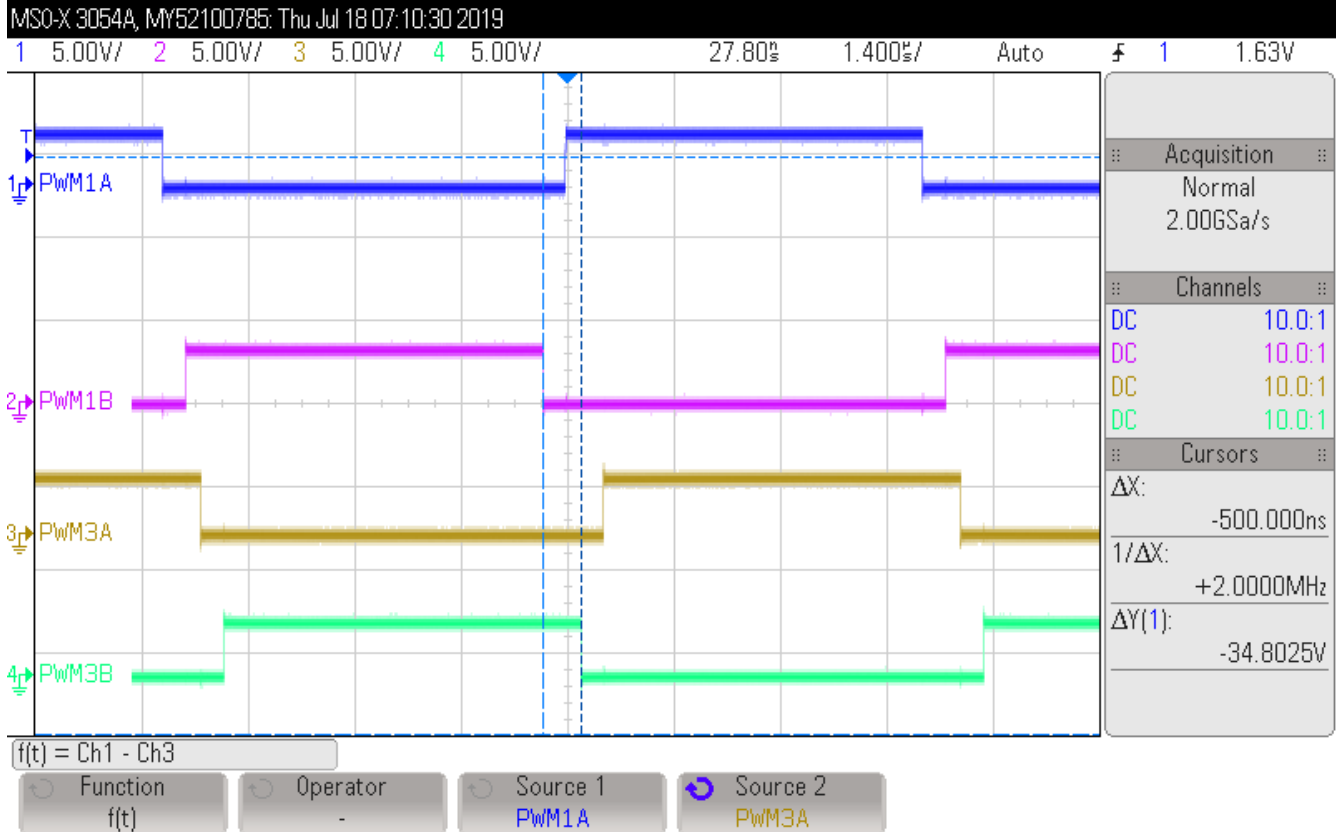
Figure 4-14. 100 kHz PWM

2. Now change the phase shift to 0.05 → 500 ns, to see more observable phase shift
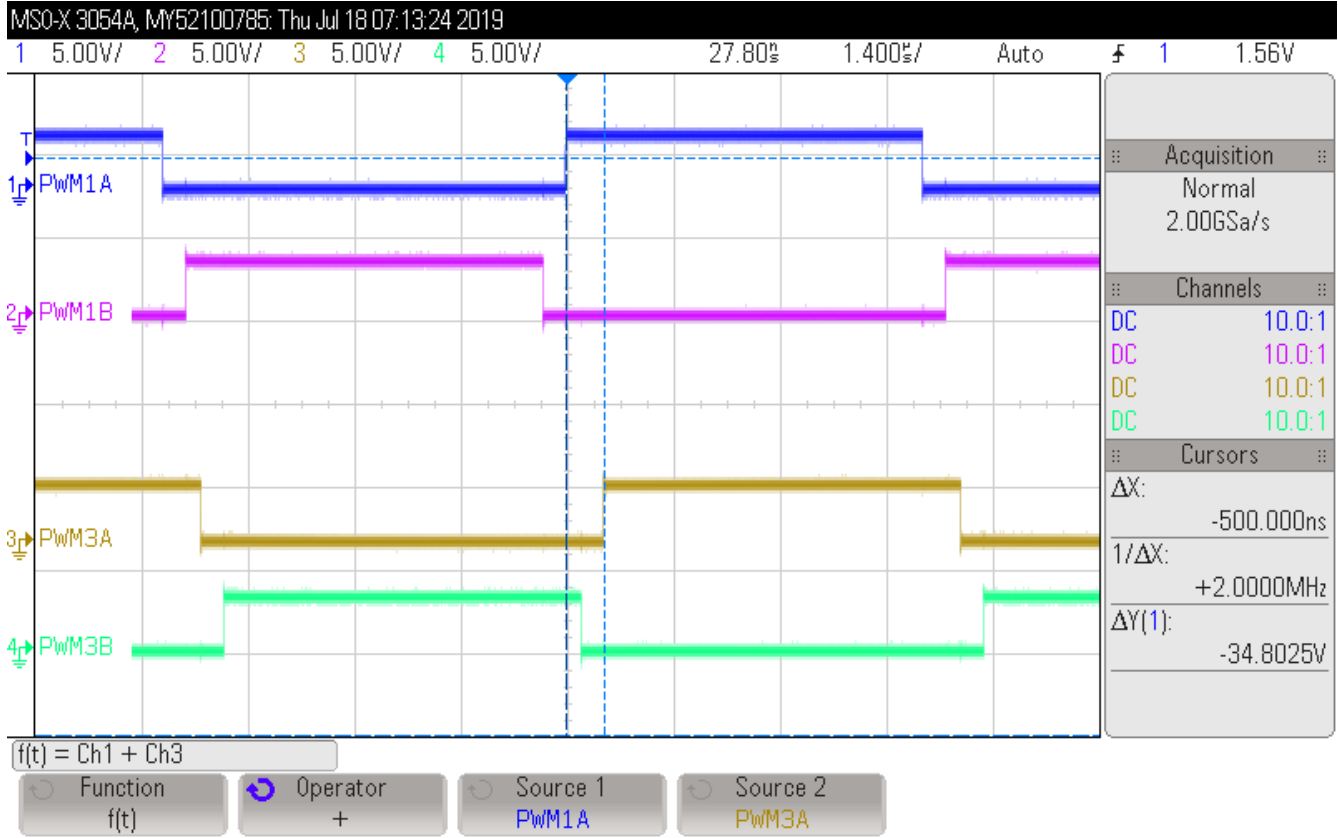
Figure 4-15. Phase Shift 500 ns

3. Phase shift matches that specified by the variable on the oscilloscope. Check for non-clock ticks, that is, sub 10-ns internals of phase shift to verify high-resolution operation. In Figure 4-16 and Figure 4-17, the phase shift is measured using the oscilloscope to be approximately 500 ns for 500-ns setpoint and approximately 502 ns for a 502-ns setpoint, small jitter approximately 1–2 ns can be the measurement error.

> **CAUTION**
> Phase shift is not recommended to be operated beyond 0.45 pu.
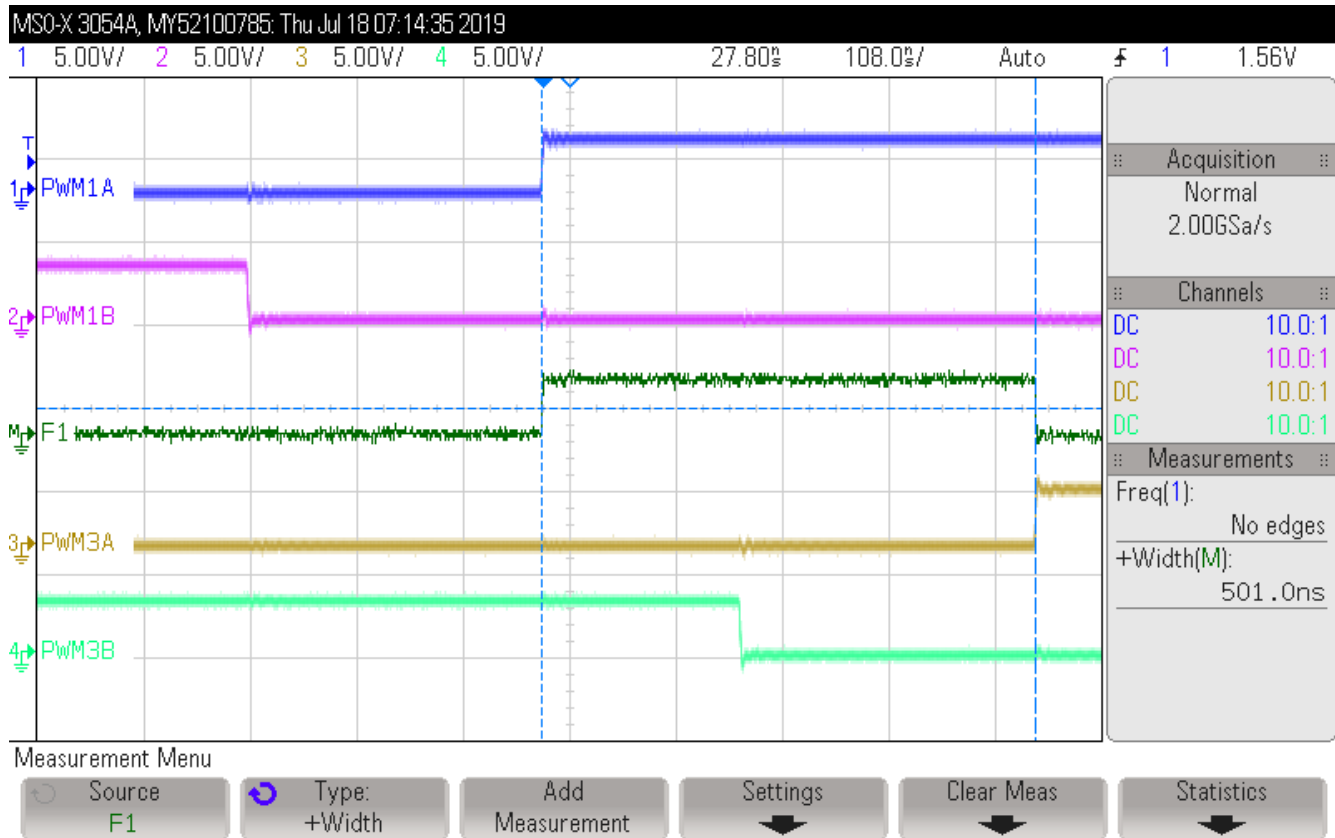
Figure 4-16. High Resolution Phase Shift 500 ns (1 ns Jitter Error)
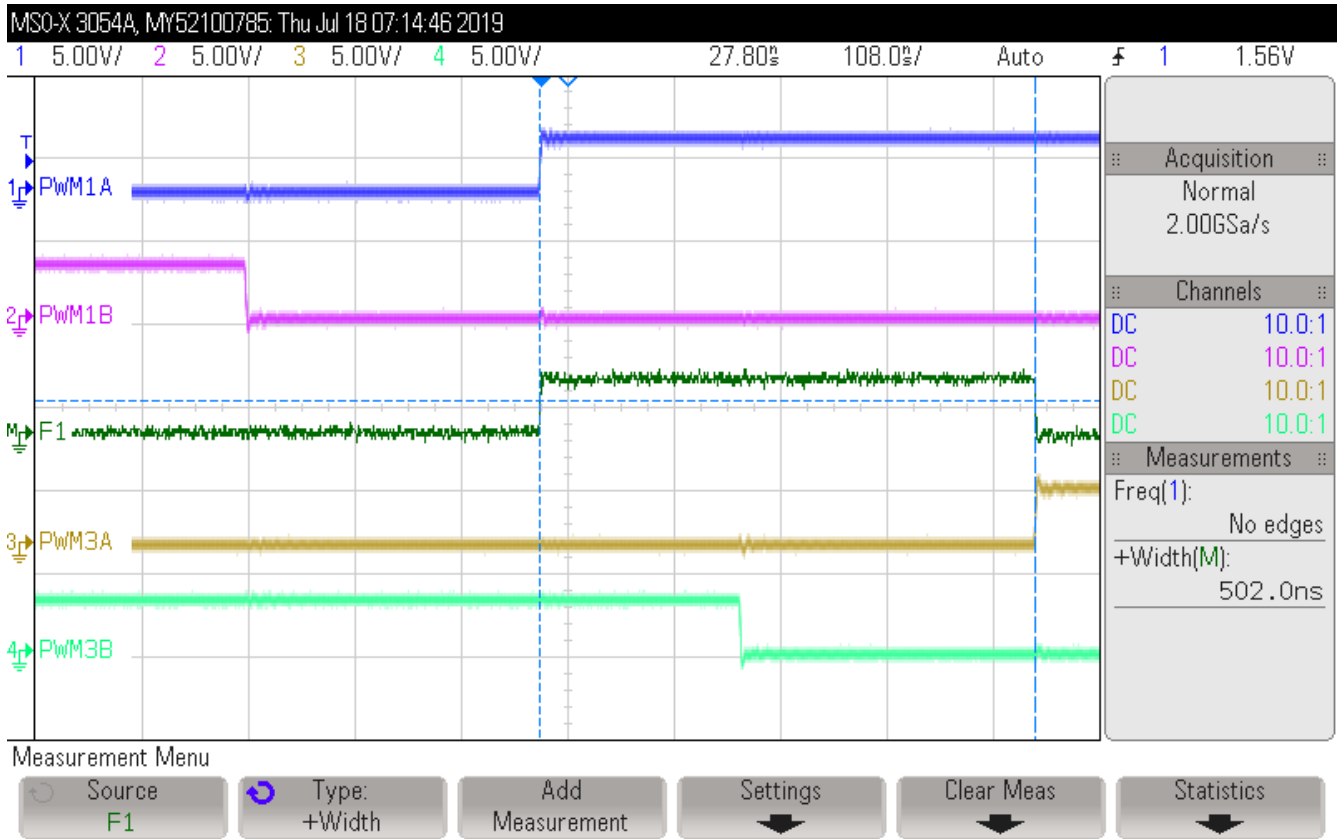
Figure 4-17. High Resolution Phase Shift 502 ns

4. Change the PWM probes to PWM1A, PWM1B, PWM2A, and PWM2B.
    –   Verify PWM1A and 2B are in sync and in phase
    –   Verify PWM1B and 2A are in sync and in phase
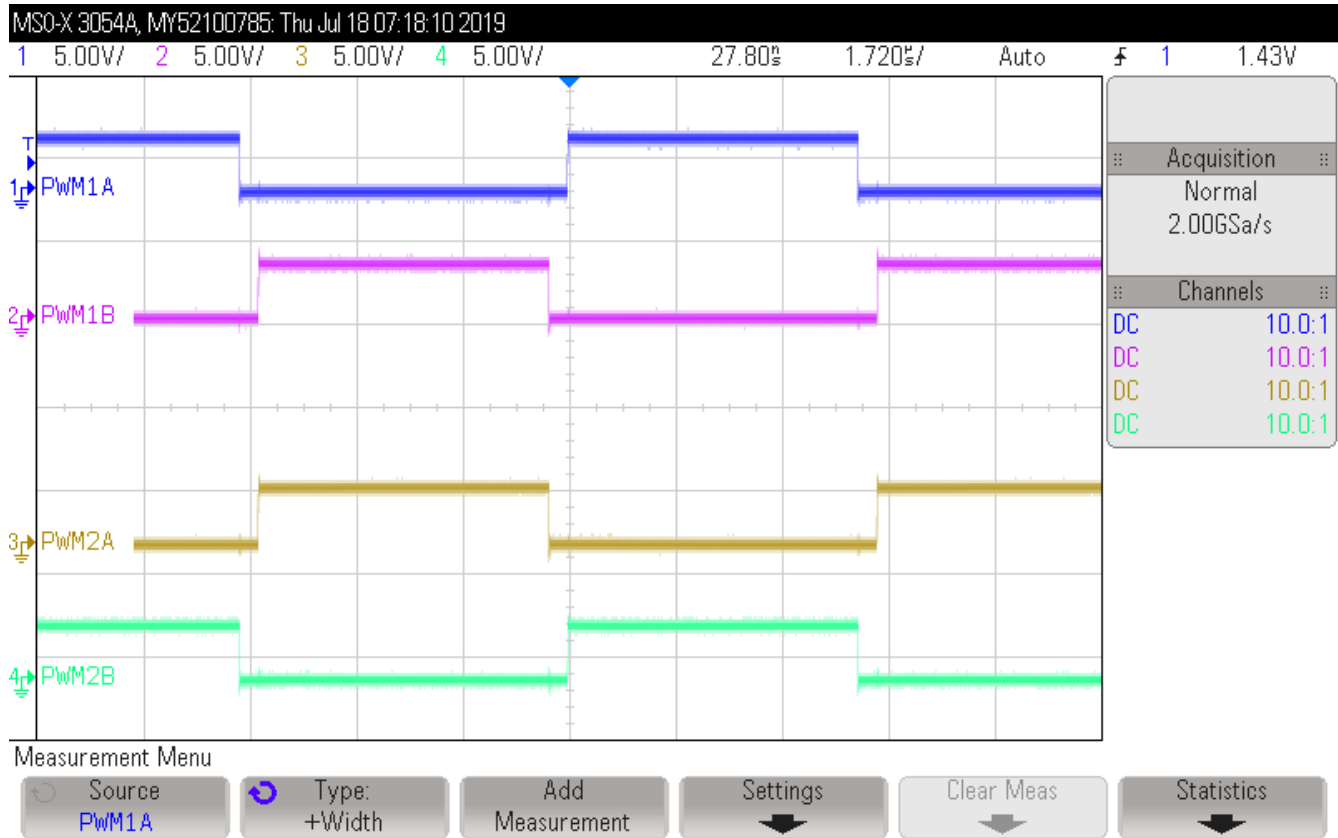
Figure 4-18. PWM in Sync

5. Verify that they remain in sync and in phase as the phase shift for sec side PWM is changed:
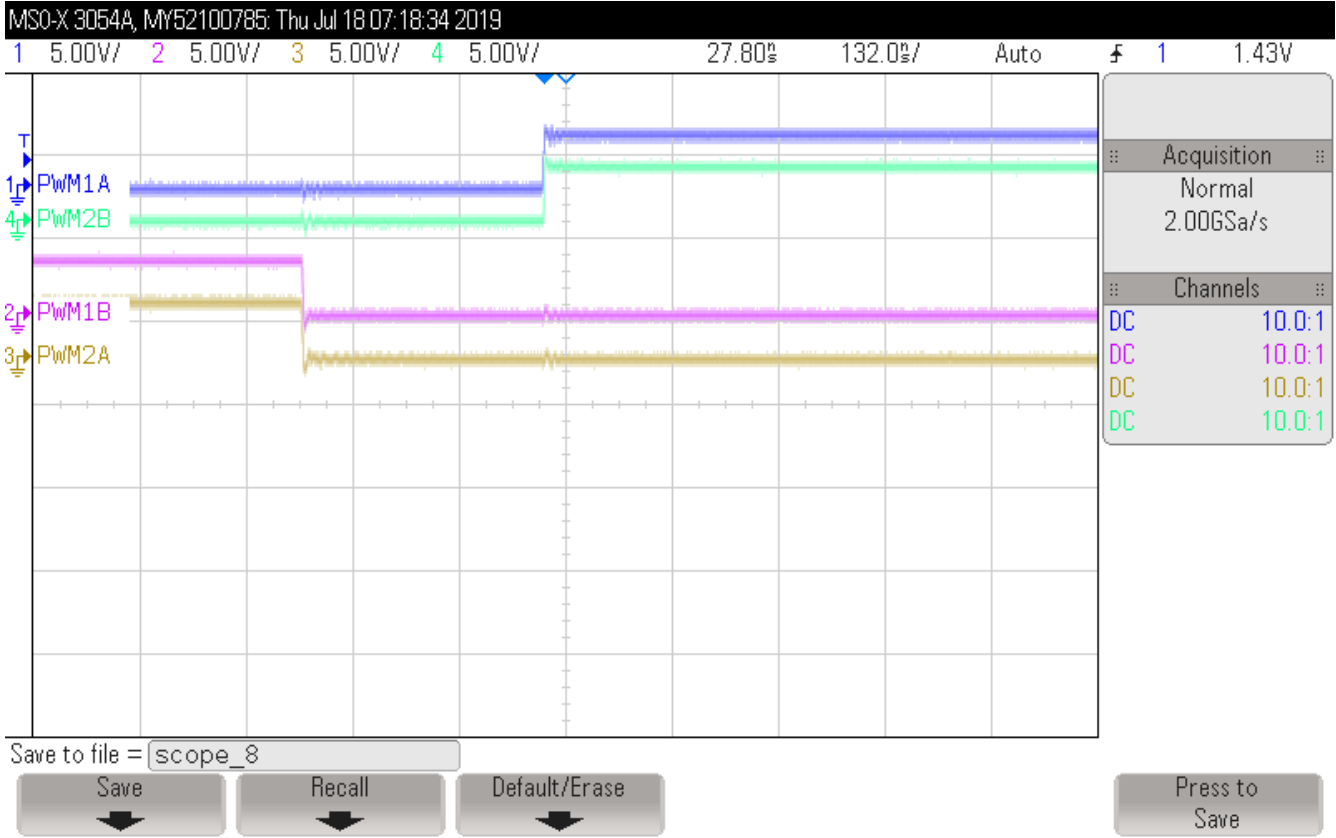
Figure 4-19. PWM in Sync With Phase Shift

4.4.2 Lab 2

In the lab 2 build, the board is excited in open-loop fashion with a specified frequency (100 kHz) and phase shift. The phase shift can be changed through the watch window. The phase shift is controlled with the DAB_pwmPhaseShiftPrimSec_pu variable. This build verifies the sensing of feedback values from the power stage, operation of the PWM gate driver, HW protection, and ensures there are no hardware issues. Additionally, calibrate the input and output voltage sensing in this build.

- **Test Setup for Lab 2**

  The hardware for this reference design is composed of the following boards:

  – One TIDA-010054 power board
  – Four TIDA-010054 gate driver cards
  – Two TIDA-01606 ISOHV sense cards
  – One TMDSCNCD280049C control card
  – Mini USB cable
  – Laptop

- **The following test equipment is needed to power and evaluate the DUT**

  – 10-kW DC source capable of delivering voltage between 700 V–800 V at required current
  – 10-kW resistive load bank
  – Power analyzer
  – Dual channel +15-V, 4-V auxiliary bench power supply
  – Oscilloscope
  – Isolated voltage probes and current probe
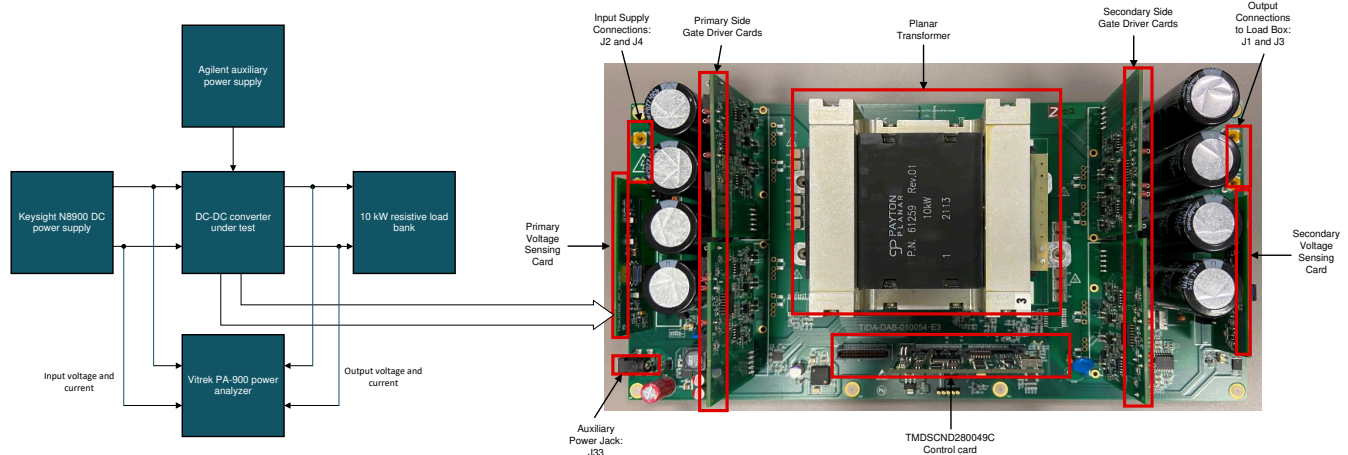
Figure 4-20. Lab 2 Test Setup

Software Setup for Lab 2

The following defines are set in the "settings.h" file for this build. The settings can be defined by selecting *Lab 2: Open Loop PWM with Protection* in the drop-down menu of Project Options from PowerSUITE GUI.

```
#if DAB_LAB == 2
#define DAB_CONTROL_RUNNING_ON C28x_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_PRIM_SEC
#define DAB_INCR_BUILD DAB_OPEN_LOOP_BUILD
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_SFRA_TYPE  DAB_SFRA_VOLTAGE
#if DAB_SFRA_TYPE == DAB_SFRA_CURRENT
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL3
#else
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL2
#endif
#endif
```

Figure 4-21. Lab 2 Software Setup

1. Run the project by clicking the green run button in CCS
2. Populate the required variables in the watch window by loading javascript ' setupdebugenv_lab2.js' in the scripting console

Expression	Type	Value	Address
(x)= DAB_buildLevel.buildLevel	enum <unnamed>	openLoopCheck	0x00008002@Data
(x)= DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_singlePhaseShiftControl	0x00008008@Data
(x)= DAB_powerFlowState.powerFlowSt	enum <unnamed>	powerFlow_BatteryCharging	0x0000800C@Data
(x)= DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008004@Data
(x)= DAB_clearTrip	long	0	0x000080C6@Data
(x)= DAB_pwmPhaseShiftPrimSecRef_p	float	0.0320000015	0x000080D6@Data
(x)= DAB_pwmPhaseShiftPrimSec_pu	float	0.0320000015	0x000080D8@Data
(x)= DAB_vPrimSensed_Volts	float	217.880859	0x00008038@Data
(x)= DAB_iPrimSensed_Amps	float	0.481933594	0x00008024@Data
(x)= DAB_vSecSensed_Volts	float	144.436905	0x0000805C@Data
(x)= DAB_iSecSensed_Amps	float	0.666992188	0x0000804E@Data
(x)= DAB_pwmFrequency_Hz	float	100000.0	0x000080CA@Data

Figure 4-22. Lab 2 Watch View Configuration

3. Enable PWM by writing "1" to the DAB_clearTrip variable
4. In the watch view, check if the DAB_vPrimSensed_Volts, DAB_iPrimSensed_Amps, DAB_vSecSensed_Volts, and DAB_iSecSensed_Amps variables are updating periodically

---
Note

Because no power is applied at this point, these are close to zero.

---

5. Now, slowly increase the input VPRIM DC voltage from 0 V to 800 V. Make sure DAB_vPrimSensed_Volts displays the correct values.
6. By default, the DAB_pwmPhaseShiftPrimSec_pu variable is set to 0.032. Vary this phase shift slowly in steps of 0.002 pu and observe the change in voltage at the output of converter. Care must be taken to not increase the phase shift very high as it can boost the output voltage greater than the input voltage and can lead to breakdown of MOSFETs at maximum applied voltage

.

- **Measure SFRA Plant for Voltage Loop**
    1. The SFRA is integrated in the **C2000Ware-DigitalPower-SDK** kit to measure the plant response which can then be used to design a compensator. Run the SFRA by clicking on the SFRA icon. The SFRA GUI opens.
    2. Select the options for the device on the SFRA GUI; for example, for F280049, select floating point. Click the *Setup Connection* button. In the pop-up window, uncheck the boot-on-connect option and select an appropriate COM port. Select the *OK* button. Return to the SFRA GUI and click the *Connect* button.
    3. The SFRA GUI connects to the device. A SFRA sweep can now be started by clicking the *Start Sweep* button. The complete SFRA sweep takes a few minutes to complete. Monitor the activity in the progress

bar on the SFRA GUI or by checking the flashing blue LED on the back of the control card, which indicates UART activity.
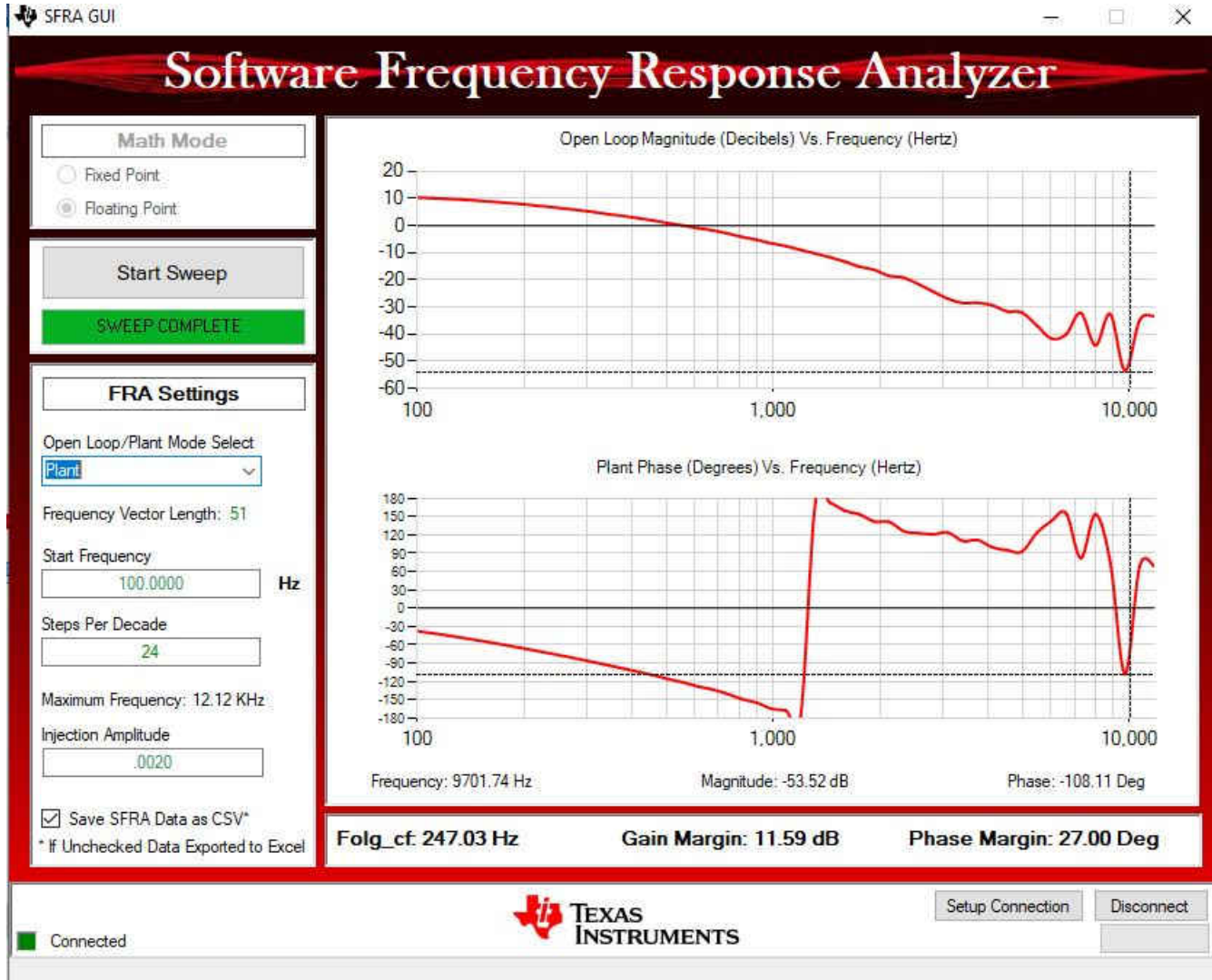
Test condition: V$_{IN}$ = 600 V, V$_{OUT}$ = 425 V, I$_{IN}$ = 4.72 A, Phase shift = 0.056, SFRA Amplitude = 0.002

Figure 4-23. Lab 2 SFRA Plant Plot for the Open Voltage Loop Test

4. The Frequency Response Data ("SFRA.csv") is saved in the project folder, under an SFRA Data Folder, and is time-stamped with the time of the SFRA run. SFRA can be run at different frequency setpoints to cover the range of operation of the system. A compensator is designed using these measured plots through compensator designer.

    Inside ISR1, the SFRA injects small signal perturbations in phase and observes the sensed output voltage variations. The following lines of code inside the dab.h file perform the SFRA signal injection and collection.

```
        #else
            DAB_pwmPeriod_pu = DAB_pwmPeriodRef_pu;
            DAB_pwmPhaseShiftPrimSec_pu =
                    DAB_SFRA_INJECT(DAB_pwmPhaseShiftPrimSecRef_pu);
        #endif

    #else
        DAB_SFRA_COLLECT((float32_t*)&DAB_pwmPhaseShiftPrimSec_pu ,
                    (float32_t*)&DAB_vSecSensed_pu);
    #endif
```

Figure 4-24. Lab 2 Code for SFRA Signal Injection

- **Measure SFRA Plant for Current Loop**
  1. Follow the same steps as in voltage loop to get started with SFRA measurement for current loop.
  2. In the PowerSUITE GUI under SFRA tab, choose "current" prior to running the SFRA current loop.

```
#define DAB_SFRA_TYPE   DAB_SFRA_CURRENT
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL3
```

Figure 4-25. Lab 2 Code Defines SFRA Current Loop

3. Inside ISR1, the SFRA injects small signal perturbations in phase and observes the sensed output current variations. The following lines of code inside the dab.h file perform the SFRA signal injection and collection.

```
        #else
            DAB_pwmPeriod_pu = DAB_pwmPeriodRef_pu;
            DAB_pwmPhaseShiftPrimSec_pu =
                    DAB_SFRA_INJECT(DAB_pwmPhaseShiftPrimSecRef_pu);
        #endif

    #if DAB_SFRA_TYPE != DAB_SFRA_DISABLED
        #if DAB_SFRA_TYPE == DAB_SFRA_CURRENT
            DAB_SFRA_COLLECT((float32_t *)&DAB_pwmPhaseShiftPrimSec_pu,
                        (float32_t *)&DAB_iSecSensed_pu);
```

Figure 4-26. Lab 2 Code for SFRA Signal Injection

4. Measure the plant response from SFRA GUI. The open loop and plant response are stored in the file named 'SFRA.csv'. Use this file to tune the compensator for the current loop.
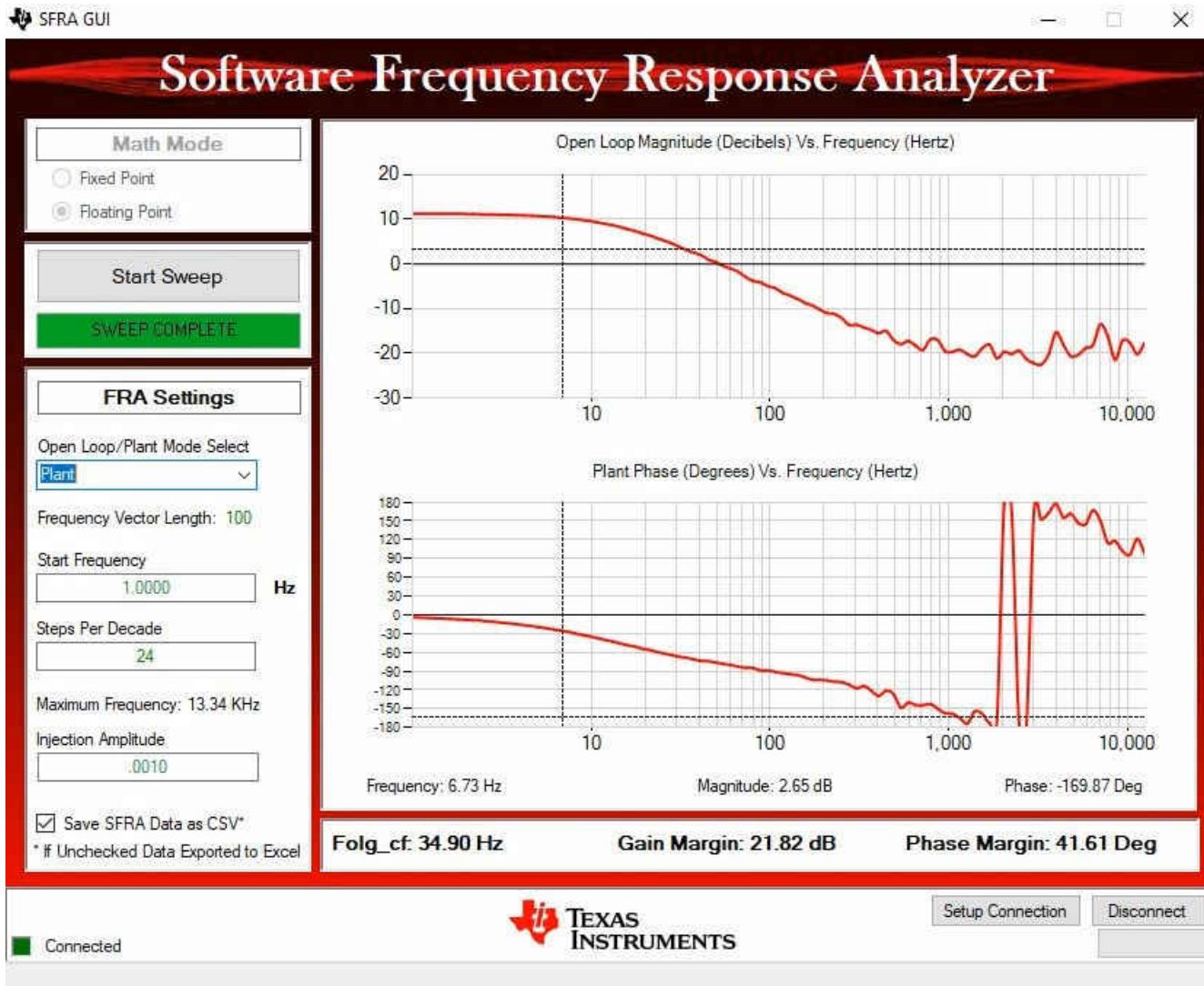
Figure 4-27. Lab 2 SFRA Plant Plot for the Open Current Loop Test

---

Note

The current is sensed by AMC3301 at the battery (load) side

- **Protection validation**

  The limits for overcurrent and overvoltage protection can be modified from PowerSUITE GUI.

```
#define DAB_ISEC_TRIP_LIMIT ((float32_t) 8.0)
#define DAB_IPRIM_TRIP_LIMIT ((float32_t) 1.5)
#define DAB_IPRIM_TANK_TRIP_LIMIT ((float32_t)35.0)
#define DAB_VSEC_TRIP_LIMIT ((float32_t)500)
```

Note

Secondary tank current and Primary overvoltage protection are not supported in the current HW.

Set the limits to a lower value and adjust the source, the load, or both to exceed the thresholds to validate the trips.
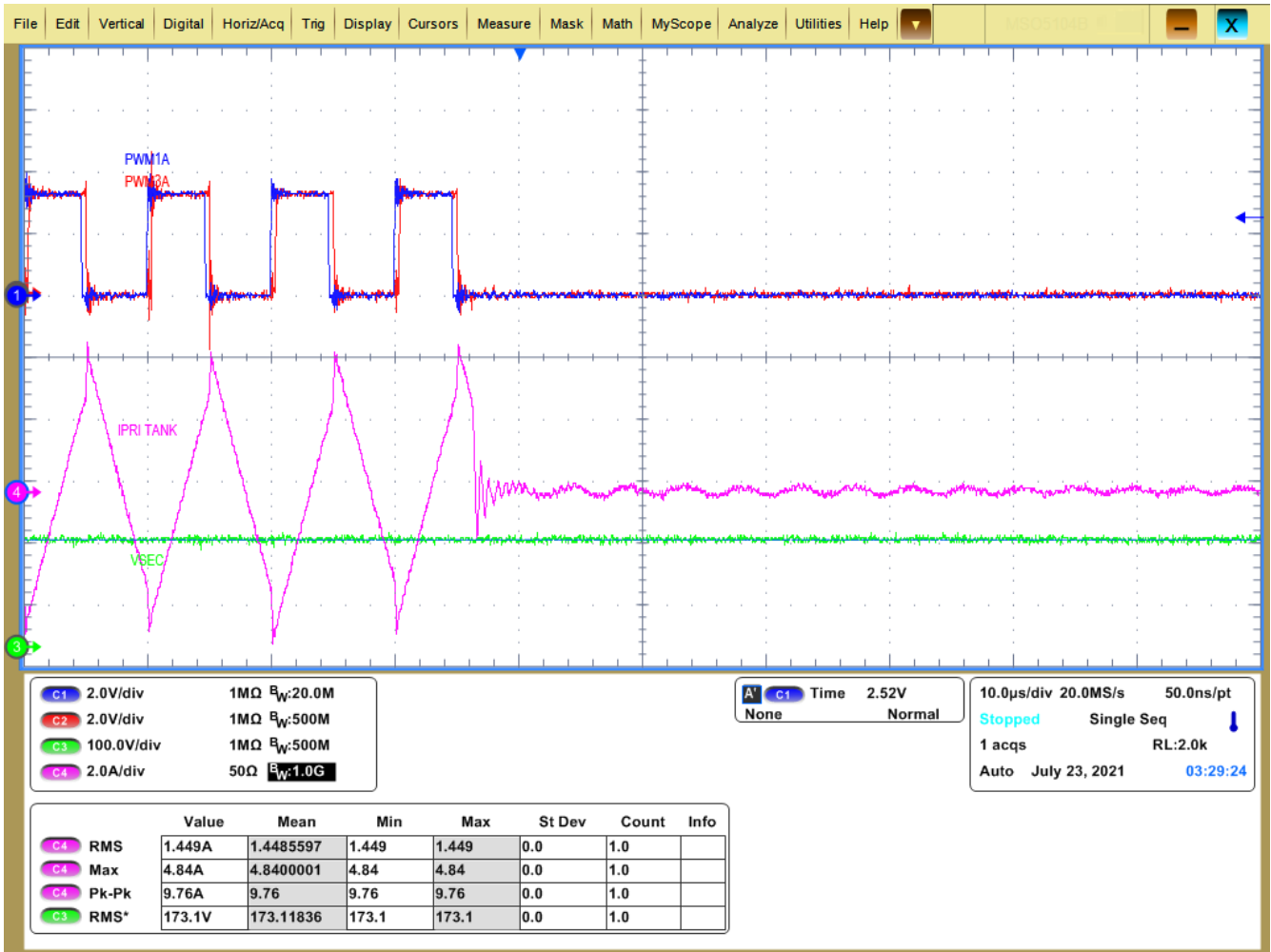
Primary - tank overcurrent protection, limit set = 4 A

Figure 4-28. Lab 2 Primary - Tank Overcurrent Protection
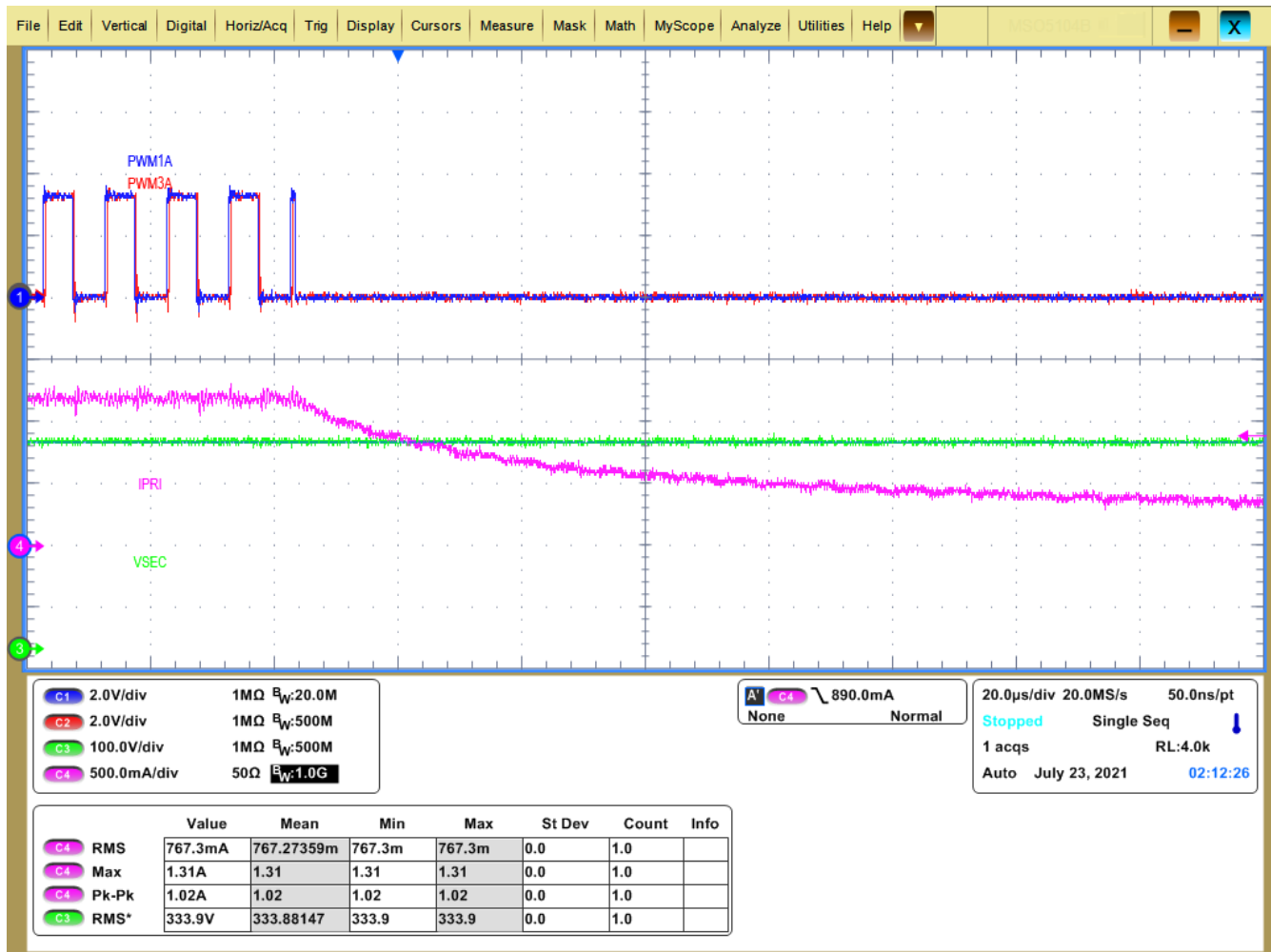
Primary (input) overcurrent protection, limit set = 1 A

Figure 4-29. Lab 2 Primary (Input) Overcurrent Protection
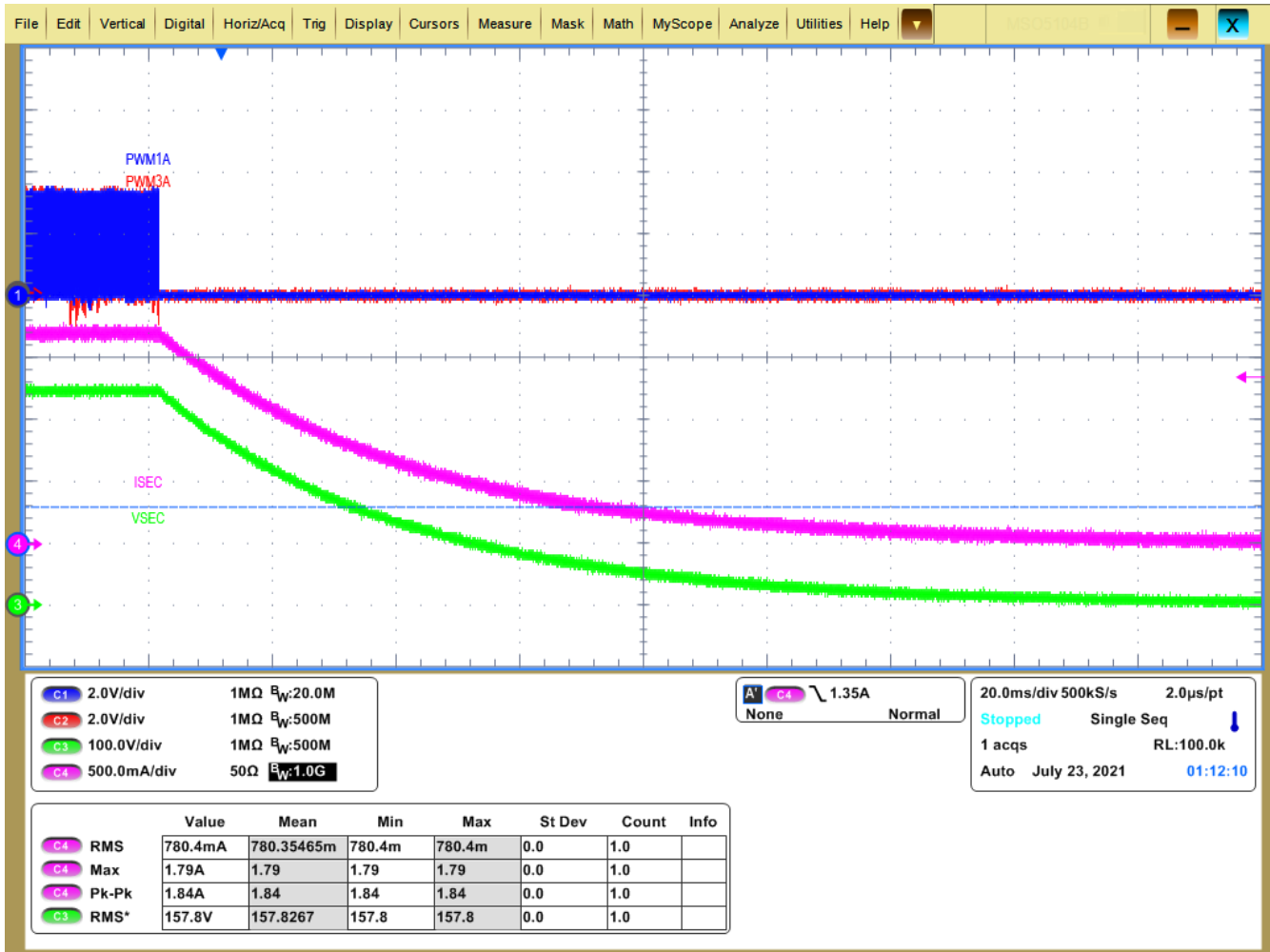
Secondary (resistive load) overcurrent protection, limit set = 1.5 A

Figure 4-30. Lab 2 Secondary (Resistive Load) Overcurrent Protection

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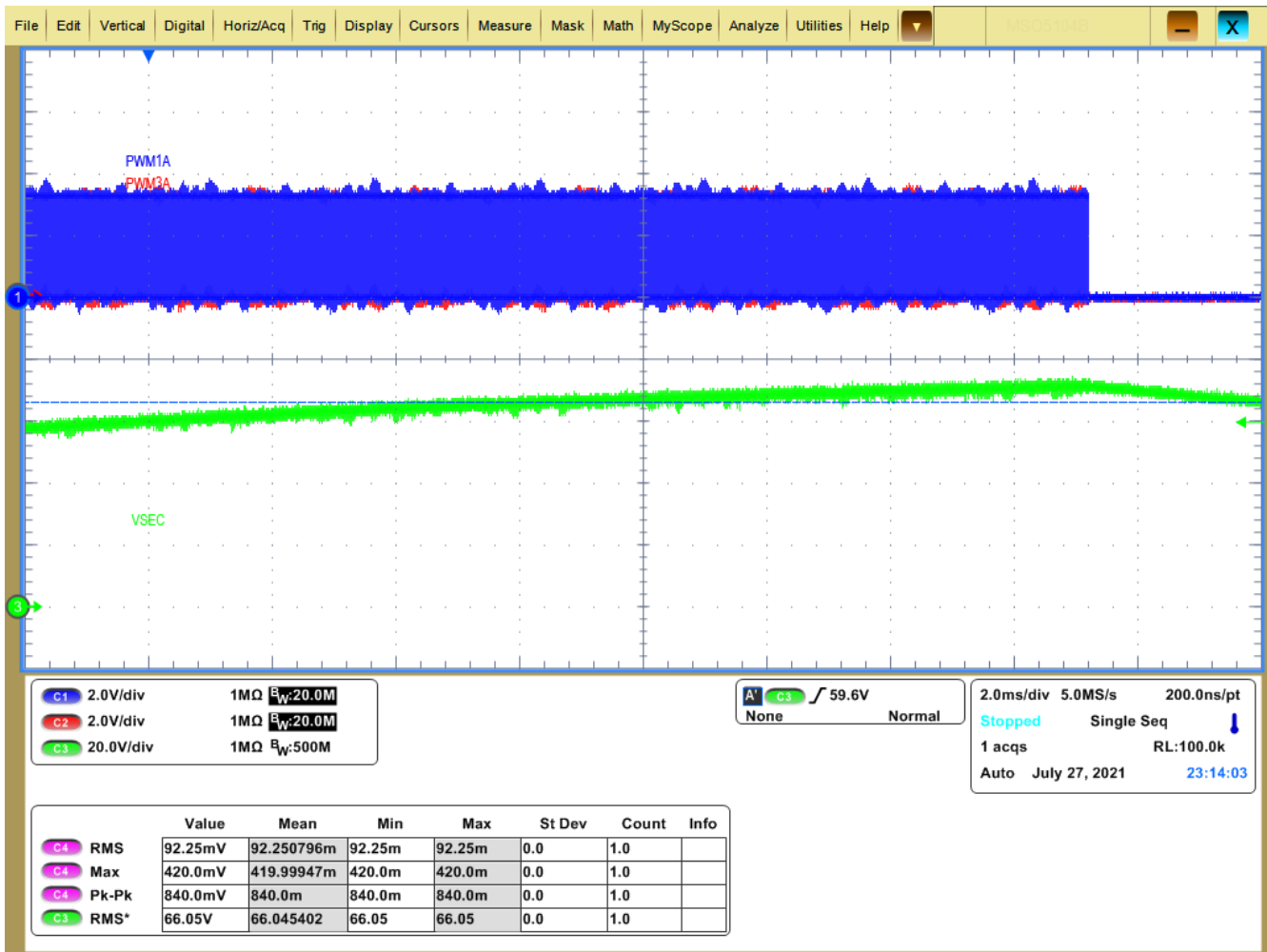
DAB_VSEC_TRIP_LIMIT = 75 V

Figure 4-31. Lab 2 Secondary Overvoltage Protection
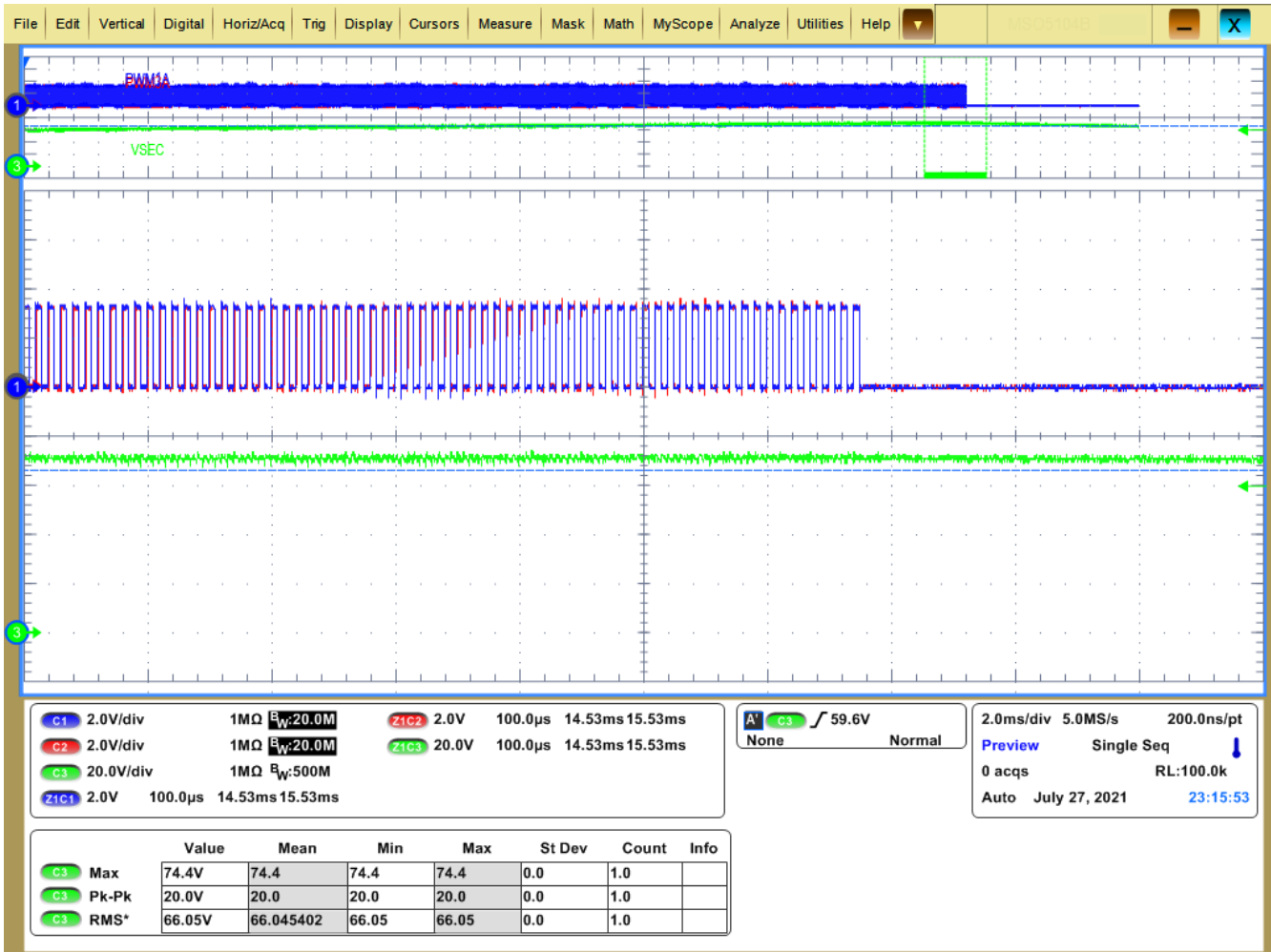
DAB_VSEC_TRIP_LIMIT = 75 V (Zoomed In)

Figure 4-32. Lab 2 Secondary Overvoltage Protection(Zoomed In)

The previous waveforms show PWM is shut off by the comparator sub-system during fault events. The type of fault is displayed in the watch window (Figure 4-33) through variable "DAB_tripFlag". The trip can be reset by selecting "noTrip" under the drop-down menu and re-enabling the PWM by writing "1" to the DAB_clearTrip variable. Make sure the fault condition is removed before re-enabling the PWM.

Figure 4-33. Lab 2-14

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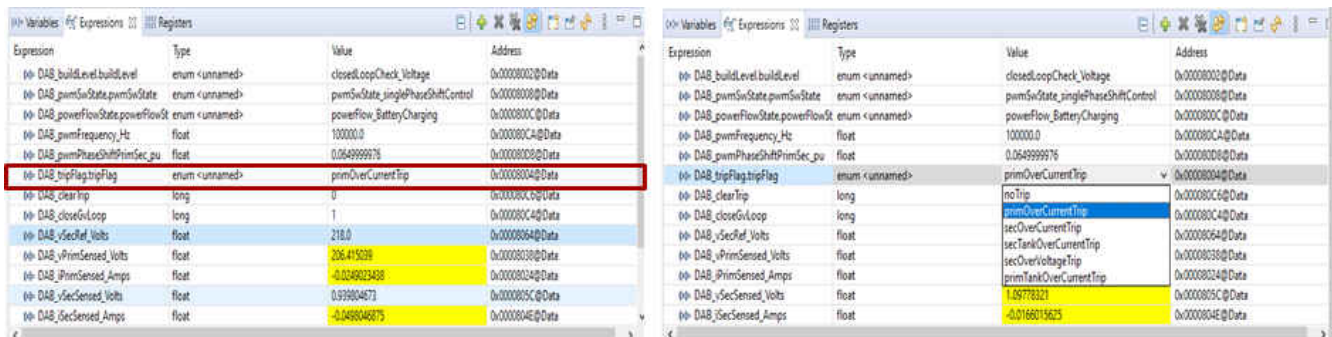
4.4.3 Lab 3

In the lab 3 build, the board is excited in secondary voltage close-loop (DAB_vSecSensed_Volts).

This lab runs the voltage mode compensator, obtain open-loop transfer function of plant from SFRA, and design compensator for the plant in compensator design tool.

Launch the compensation designer which prompts to select a valid SFRA data file. Import the SFRA data from the run in lab 2 into the compensation designer to design a 2P2Zcompensator. Keep more margins during this iteration of the design to ensure that when the loop is closed, the system is stable. The following coefficient values are hard-coded in the SW. The compensation designer GUI gives information about the stability of the loop, gain margin, phase margin, and bandwidth of the loop. The coefficients can be modified in the compensation designer GUI.

```
#define DAB_GV_2P2Z_A1 ((float32_t) -1.8756666)
#define DAB_GV_2P2Z_A2 (float32_t) 0.8756666
#define DAB_GV_2P2Z_B0 (float32_t) 3.0092688
#define DAB_GV_2P2Z_B1 ((float32_t) -5.8788593)
#define DAB_GV_2P2Z_B2 (float32_t) 2.8696427
```
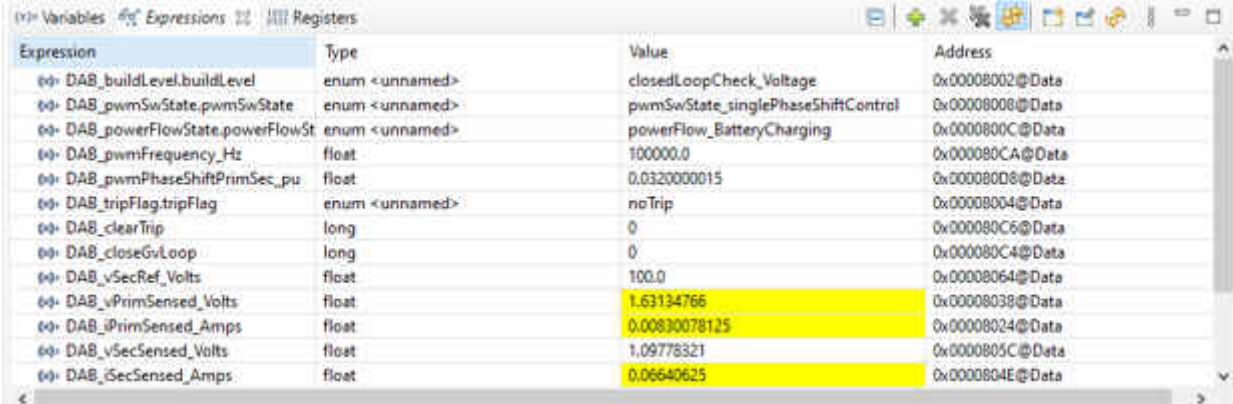
- **Test Setup for Lab 3 (Closed Voltage Loop - Vsec)**

    Compile the project by selecting *Lab 3: Closed Loop Voltage with Resistive Load* in the drop-down menu of Project Options from PowerSUITE GUI. Ensure current and voltage limits are set per operating conditions.

```
#if DAB_LAB == 3
#define DAB_CONTROL_RUNNING_ON C28X_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_PRIM_SEC
#define DAB_INCR_BUILD DAB_CLOSED_LOOP_BUILD
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_CONTROL_MODE DAB_VOLTAGE_MODE
#define DAB_SFRA_TYPE 2
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL2
#endif
```

Use the following steps to run voltage close loop:

1. Run the project by clicking green run button in CCS
2. Populate the required variables in the watch window by loading javascript ' setupdebugenv_lab3.js' in the scripting console

Figure 4-34. Lab 3 Watch View Configuration

3. Enable PWM by writing "1" to the DAB_clearTrip variable

4. In the watch view, check if the DAB_vPrimSensed_Volts, DAB_iPrimSensed_Amps, DAB_vSecSensed_Volts, and DAB_iSecSensed_Amps variables are updating periodically
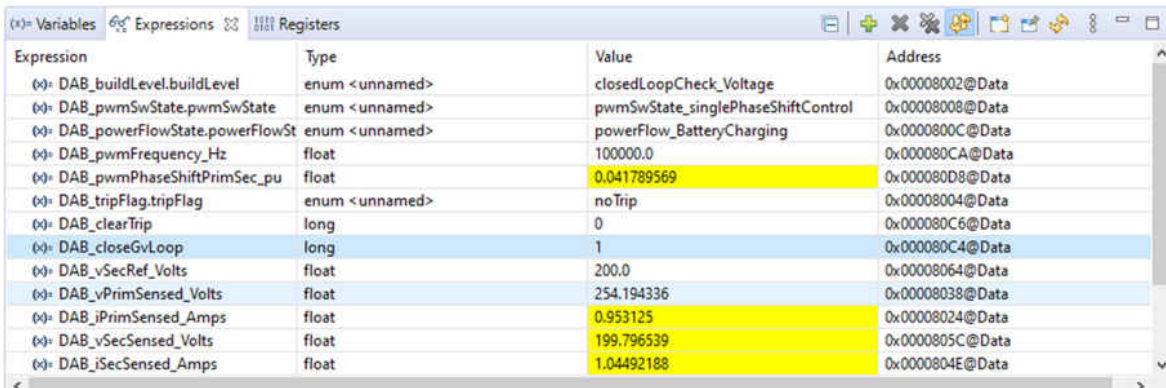
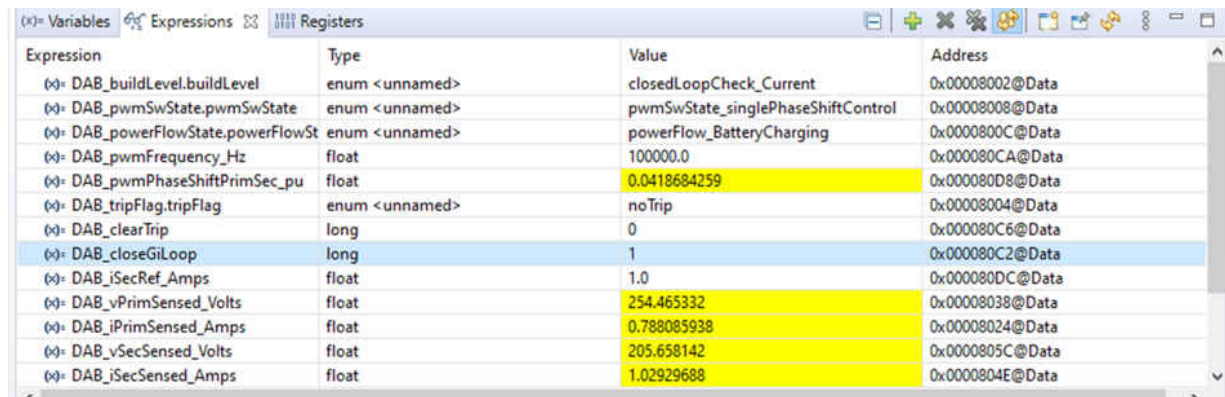| Expression	Type	Value	Address
(×)= DAB_buildLevel.buildLevel	enum <unnamed>	closedLoopCheck_Voltage	0x00008002@Data
(×)= DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_singlePhaseShiftControl	0x00008008@Data
(×)= DAB_powerFlowState.powerFlowSt	enum <unnamed>	powerFlow_BatteryCharging	0x0000800C@Data
(×)= DAB_pwmFrequency_Hz	float	100000.0	0x000080CA@Data
(×)= DAB_pwmPhaseShiftPrimSec_pu	float	0.041789569	0x000080D8@Data
(×)= DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008004@Data
(×)= DAB_clearTrip	long	0	0x000080C6@Data
(×)= DAB_closeGvLoop	long	1	0x000080C4@Data
(×)= DAB_vSecRef_Volts	float	200.0	0x00008064@Data
(×)= DAB_vPrimSensed_Volts	float	254.194336	0x00008038@Data
(×)= DAB_iPrimSensed_Amps	float	0.953125	0x00008024@Data
(×)= DAB_vSecSensed_Volts	float	199.796539	0x0000805C@Data
(×)= DAB_iSecSensed_Amps	float	1.04492188	0x0000804E@Data

Figure 4-35. Lab 3 Watch View - Enable Closed Loop

5. Set the output voltage by writing to DAB_vSecRef_Volts (in this example 200Vdc)
6. Enable closed loop operation by writing "1" to the DAB_closeGvLoop variable. The controller automatically adjusts the phase shift from default 0.032 to 0.04178, depending upon the operating conditions to generate secondary output voltage to match with that of DAB_vSecRef_Volts.

Note

In the software the maximum phase shift is limited to 0.065 as a safety precaution. Adjust the primary voltage to stay within the phase shift limits and still generate the required secondary voltage. Alternatively, the maximum allowed phase shift can be modified to 0.15 in the code.

---

7. Slowly increase the input VPRIM DC voltage and adjust DAB_vSecRef_Volts accordingly to reach to the required operating point
8. Test the closed-loop operation by varying DAB_vSecRef_Volts from 400 V to 500 V. Observe that the DAB_vSecSensed_Volts tracks this command reference.

- **Frequency response of closed loop voltage**
  1. Run the SFRA by clicking on the SFRA icon. The SFRA GUI opens.
  2. Select the options for the device on the SFRA GUI; for example, for F280049, select floating point. Click the *Setup Connection* button. In the pop-up window, uncheck the boot-on-connect option and select an appropriate COM port. Select the *OK* button. Return to the SFRA GUI and click the *Connect* button.
  3. The SFRA GUI connects to the device. An SFRA sweep can now be started by clicking the *Start Sweep* button. The complete SFRA sweep takes a few minutes to finish. Monitor the activity in the progress bar on the SFRA GUI or by checking the flashing blue LED on the back of the control card, which indicates UART activity.

  The bode plot in Figure 4-36 is captured using a DF22 compensator.
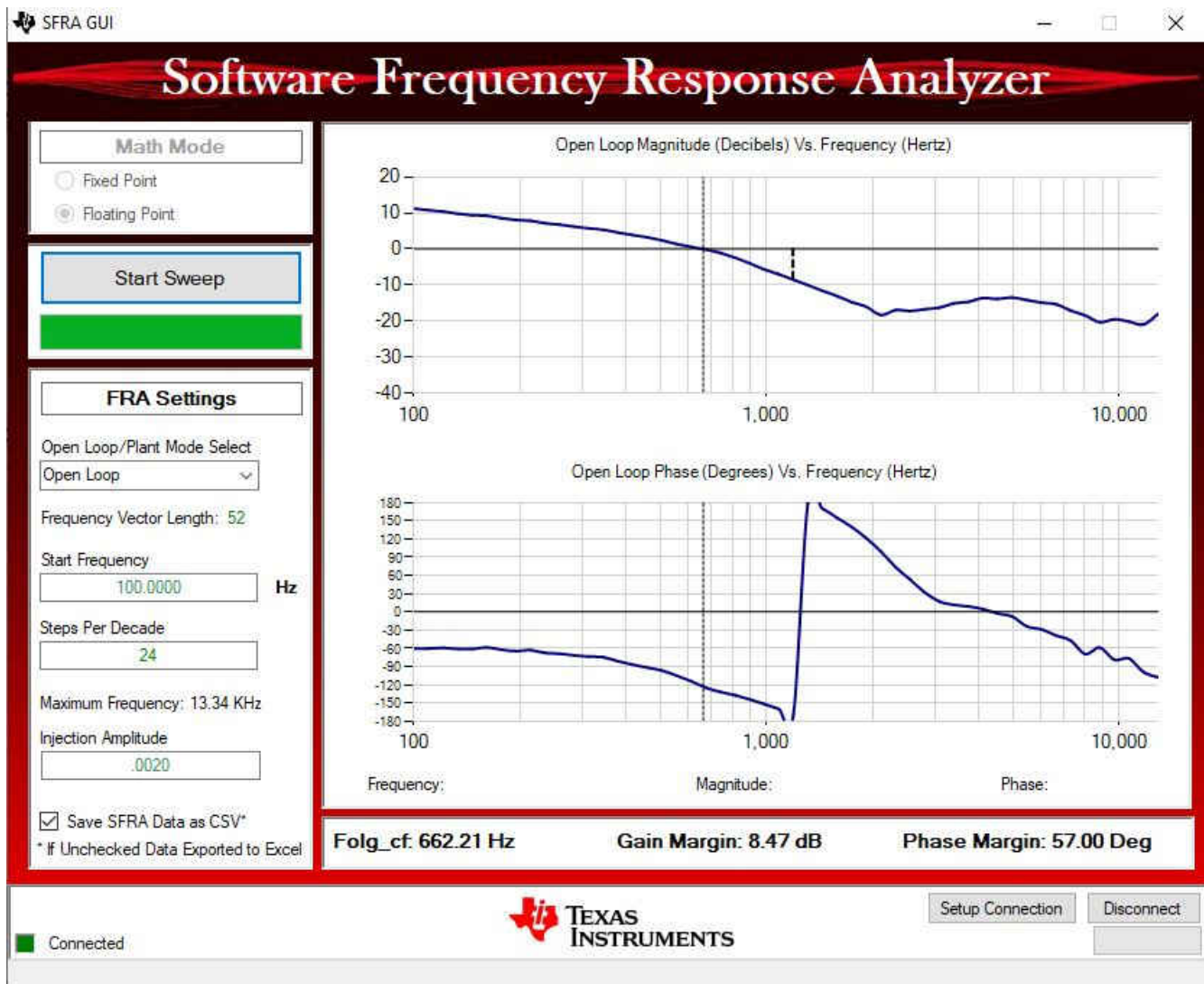
Test condition: V_{IN} = 600 V, I_{IN} = 4.78 A, V_{OUT} = 425 V, SFRA Amplitude = 0.002

Figure 4-36. Lab 3 SFRA Open Loop Plot for the Closed Voltage Loop
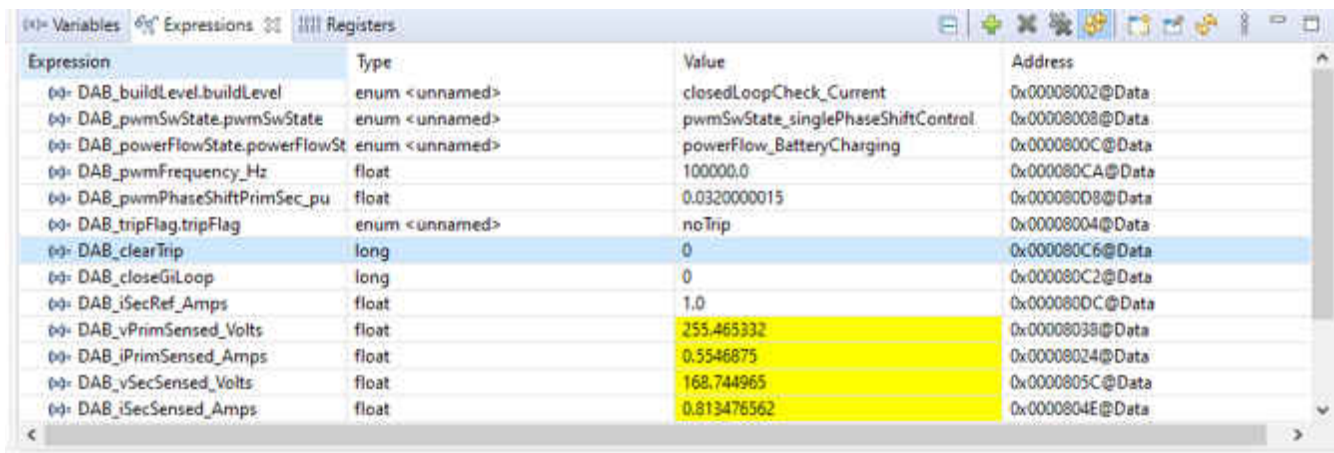
4.4.4 Lab 4

- **Test Setup for Lab 4 (Closed Current Loop - Isec)**

    Compile the project by selecting *Lab 4: Closed Loop Current with Resistive Load* in the drop-down menu of Project Options from PowerSUITE GUI. Ensure current/voltage limits are set per operating conditions.

```
#if DAB_LAB == 4
#define DAB_CONTROL_RUNNING_ON C28X_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_PRIM_SEC
#define DAB_INCR_BUILD DAB_CLOSED_LOOP_BUILD
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_CONTROL_MODE DAB_CURRENT_MODE
#define DAB_SFRA_TYPE 1
#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL1
#endif
```

1. Run the project by clicking green run button in CCS
2. Populate the required variables in the watch window by loading javascript ' setupdebugenv_lab4.js' in the scripting console

Figure 4-37. Lab 4 Watch View Configuration

3. Enable PWM by writing "1" to the DAB_clearTrip variable
4. In the watch view, check if the DAB_vPrimSensed_Volts, DAB_iPrimSensed_Amps, DAB_vSecSensed_Volts, and DAB_iSecSensed_Amps variables are updating periodically
5. Set the output current by writing to DAB_iSecRef_Amps (in this example 1Adc)
6. Enable closed loop operation by writing "1" to the DAB_closeGiLoop variable. The controller automatically adjusts the phase shift from default 0.032 to 0.04186 depending upon the operating conditions to generate secondary output current to match with that of DAB_iSecRef_Amps.

Note

In the software the maximum phase shift is limited to 0.065 as a safety precaution. Please adjust the primary voltage to stay within the phase shift limits and still generate the required secondary current. Alternatively the maximum allowed phase shift can be modified to 0.15 in the code.

Figure 4-38. Lab 4 Watch View - Enable Closed Loop

7. Now, slowly increase the input VPRIM DC voltage and adjust DAB_iSecRef_Amps accordingly to reach to the required operating point.


Note

Ensure to limit the secondary current is limited to a safe value depending upon the output load. High impedance load can lead to dangerous secondary voltage which can destroy the board. Make sure secondary over voltage protection is enabled and the threshold is set to safe value.

```
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_VSEC_TRIP_LIMIT ((float32_t)500)
#define DAB_BOARD_PROTECTION_VSEC_OVERVOLTAGE 1
```

- **Frequency response of closed loop current**
  1. Run the SFRA by clicking on the SFRA icon. The SFRA GUI will pop up.
  2. Select the options for the device on the SFRA GUI; for example, for F280049, select floating point. Click the *Setup Connection* button. In the pop-up window, uncheck the boot-on-connect option and select an appropriate COM port. Select the *OK* button. Return to the SFRA GUI and click *Connect*.
  3. The SFRA GUI will connect to the device. A SFRA sweep can now be started by clicking "Start Sweep". The complete SFRA sweep will take a few minutes to finish. Monitor the activity in the progress bar on the SFRA GUI or by checking the flashing blue LED on the back of the control card, which indicates UART activity.

  The plot in Figure 4-39 is captured with the PI compensator (gain of 6).
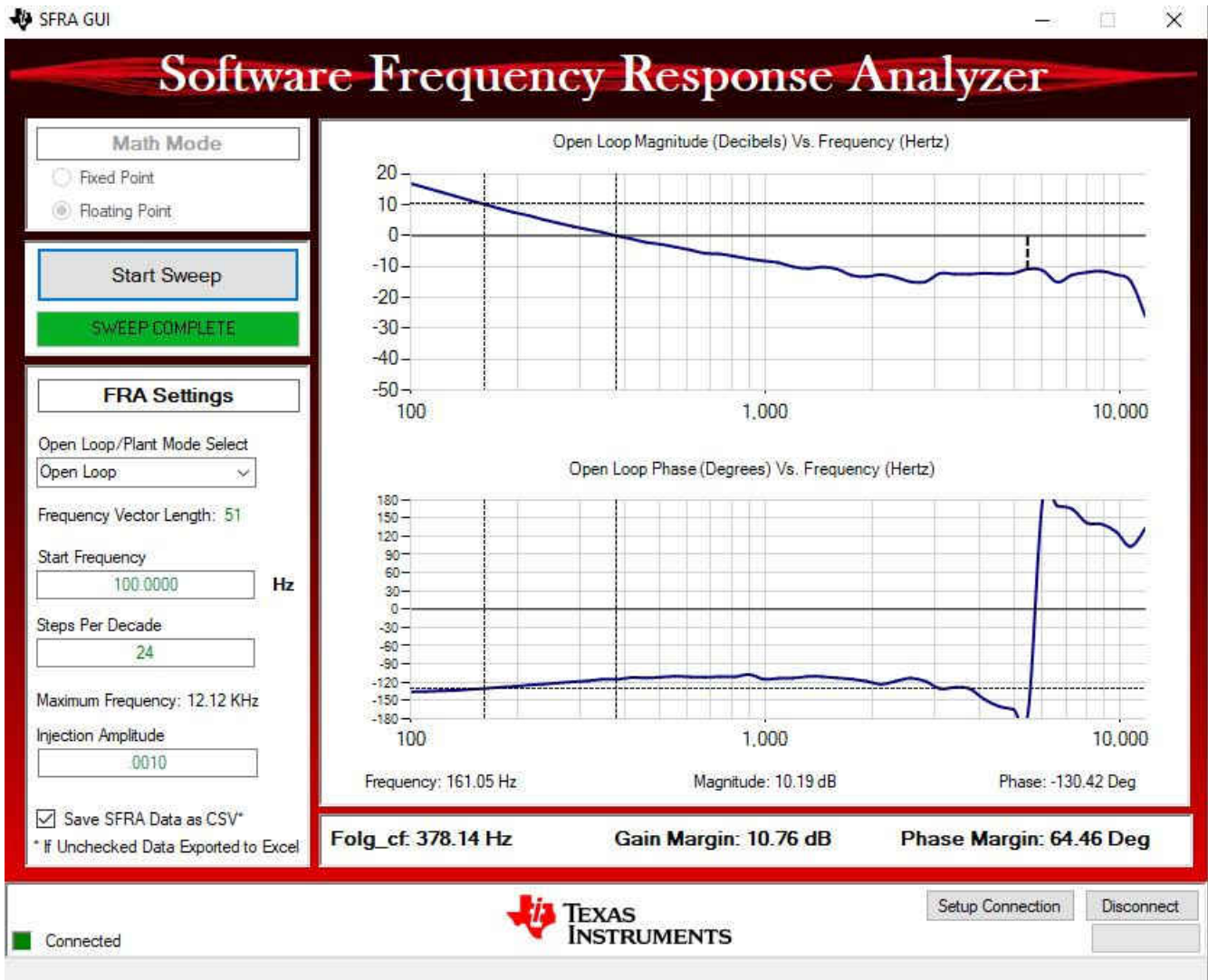
Test condition: V_{IN} = 600 V, I_{OUT} = 4.2 A, V_{OUT} = 440 V

Figure 4-39. Lab 4 SFRA Open Loop Plot for the Closed Current Loop

Current is sensed by AMC3301 at battery(load) side. PI Controller information follows:

```
#define DAB_GI_KP 6
#define DAB_GI_KI 0.0063030
#define DAB_GI_UMAX 0.06
#define DAB_GI_UMIN 0.001
#define DAB_GI_IMAX 2.0
#define DAB_GI_IMIN ((float32_t) - 2.0)
```

4.4.5 Lab 5

• Figure 4-40 shows test setup for lab 5 (Open Loop voltage - Reverse power flow).

In this setup, the DC source is connected to secondary side and the resistive load is connected to primary side.
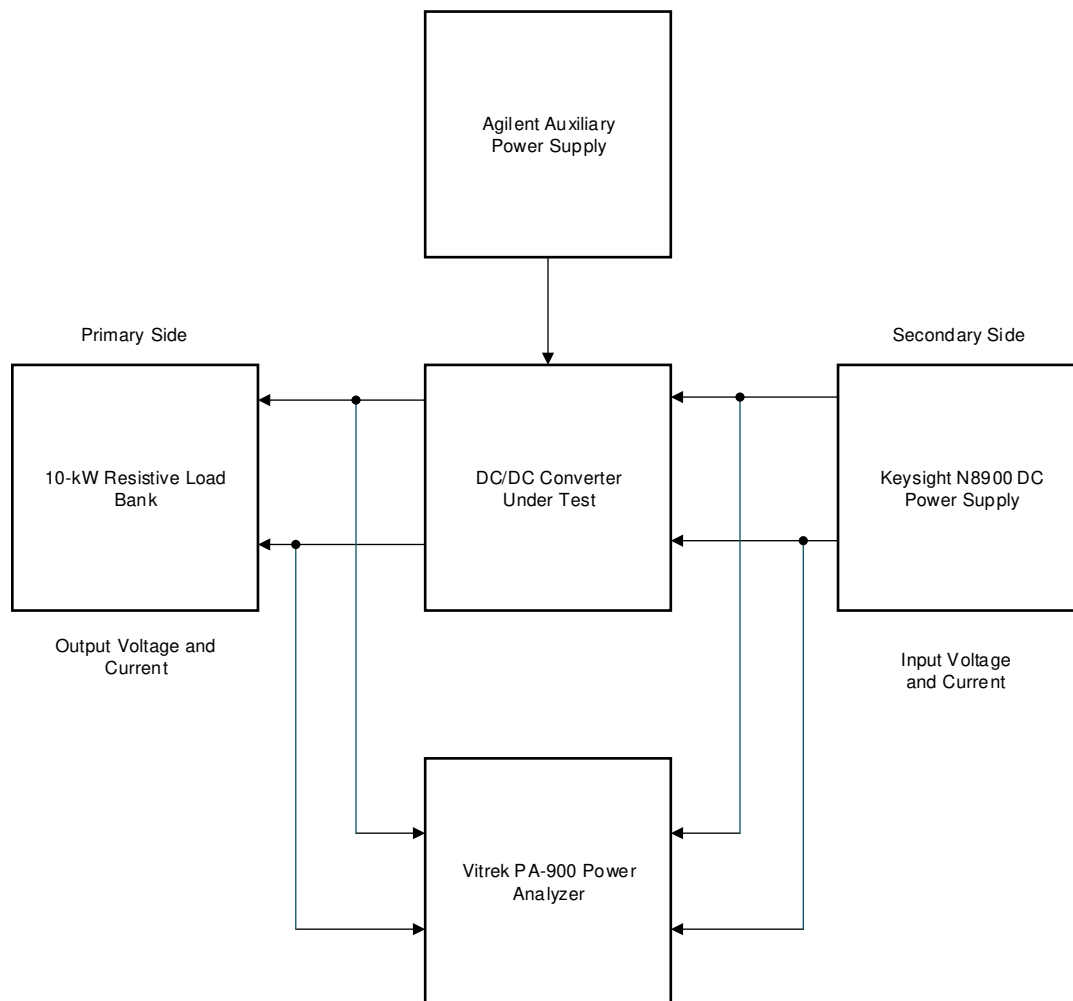
Figure 4-40. Lab 5 Test Setup

• Compile the project by selecting *Lab 5: Open Loop PWM, Sec to Prim Power Flow* in the drop-down menu of Project Options from PowerSUITE GUI. Ensure current and voltage limits are set per operating conditions.

```
#if DAB_LAB == 5
#define DAB_CONTROL_RUNNING_ON C28X_CORE
#define DAB_POWER_FLOW DAB_POWER_FLOW_SEC_PRI
#define DAB_INCR_BUILD DAB_OPEN_LOOP_BUILD
#define DAB_TEST_SETUP DAB_TEST_SETUP_RES_LOAD
#define DAB_PROTECTION DAB_PROTECTION_ENABLED
#define DAB_CONTROL_MODE DAB_VOLTAGE_MODE
#define DAB_SFRA_TYPE 0#define DAB_SFRA_AMPLITUDE (float32_t)DAB_SFRA_INJECTION_AMPLITUDE_LEVEL2
#endif
```

1. Run the project by clicking green run button in CCS
2. Populate the required variables in the watch window by loading javascript ' setupdebugenv_lab5.js' in the scripting console

Expression	Type	Value	Address
(x)= DAB_buildLevel.buildLevel	enum <unnamed>	openLoopCheck	0x00008002@Data
(x)= DAB_pwmSwState.pwmSwState	enum <unnamed>	pwmSwState_singlePhaseShiftControl	0x00008008@Data
(x)= DAB_powerFlowState.powerFlowSt	enum <unnamed>	powerFlow_BatteryDischarging	0x0000800C@Data
(x)= DAB_tripFlag.tripFlag	enum <unnamed>	noTrip	0x00008004@Data
(x)= DAB_clearTrip	long	0	0x000080C6@Data
(x)= DAB_pwmFrequency_Hz	float	100000.0	0x000080CA@Data
(x)= DAB_pwmPhaseShiftPrimSecRef_p	float	-0.0320000015	0x000080D6@Data
(x)= DAB_vPrimSensed_Volts	float	173.166504	0x00008038@Data
(x)= DAB_iPrimSensed_Amps	float	-0.87890625	0x00008024@Data
(x)= DAB_vSecSensed_Volts	float	103.191628	0x0000805C@Data
(x)= DAB_iSecSensed_Amps	float	-1.54199219	0x0000804E@Data
➕ Add new expression			

Figure 4-41. Lab 5 Watch View

3. Enable PWM by writing "1" to the DAB_clearTrip variable
4. Vary phase shift slowly in steps of 0.002 pu by writing to DAB_pwmPhaseShiftPrimSec_pu and observe the change in voltage at the output of converter.

Note
The negative sign in the phase shift value is required for the reverse power flow.

Test Conditions: V_{OUT} = 600 V_{DC}, Phase shift = –0.032, V_{IN} = 330 V_{DC}, Load = 400 Ω

Figure 4-42. Lab 5 Reverse Power Flow

- **Overcurrent Protections (Reverse Power Flow)**

    Figure 4-43 and Figure 4-44illustrate the overcurrent protections (reverse power flow).
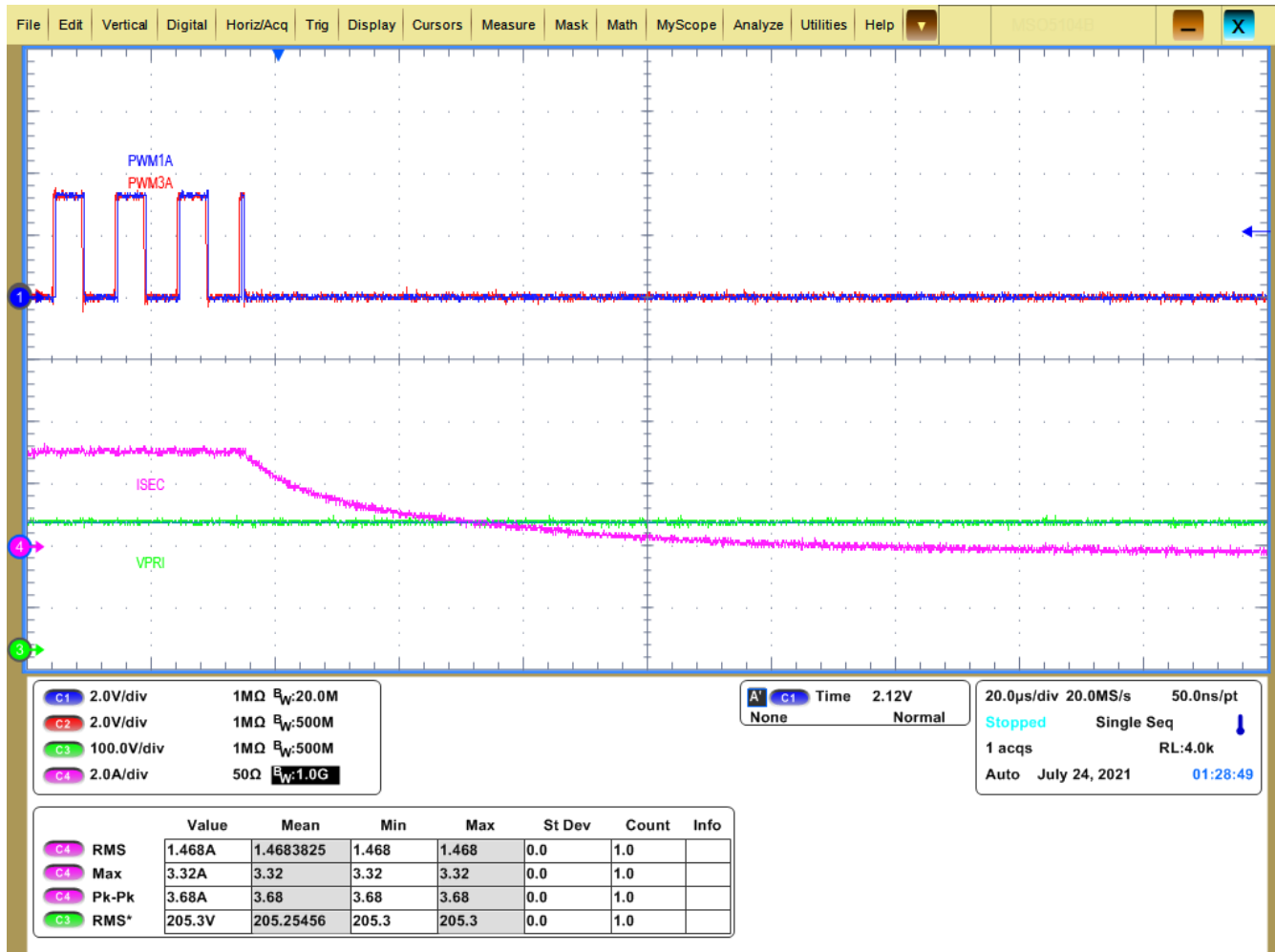
Figure 4-43. Lab 5 Reverse Power Flow Trip on Secondary (Source), Limit Set = 4 A
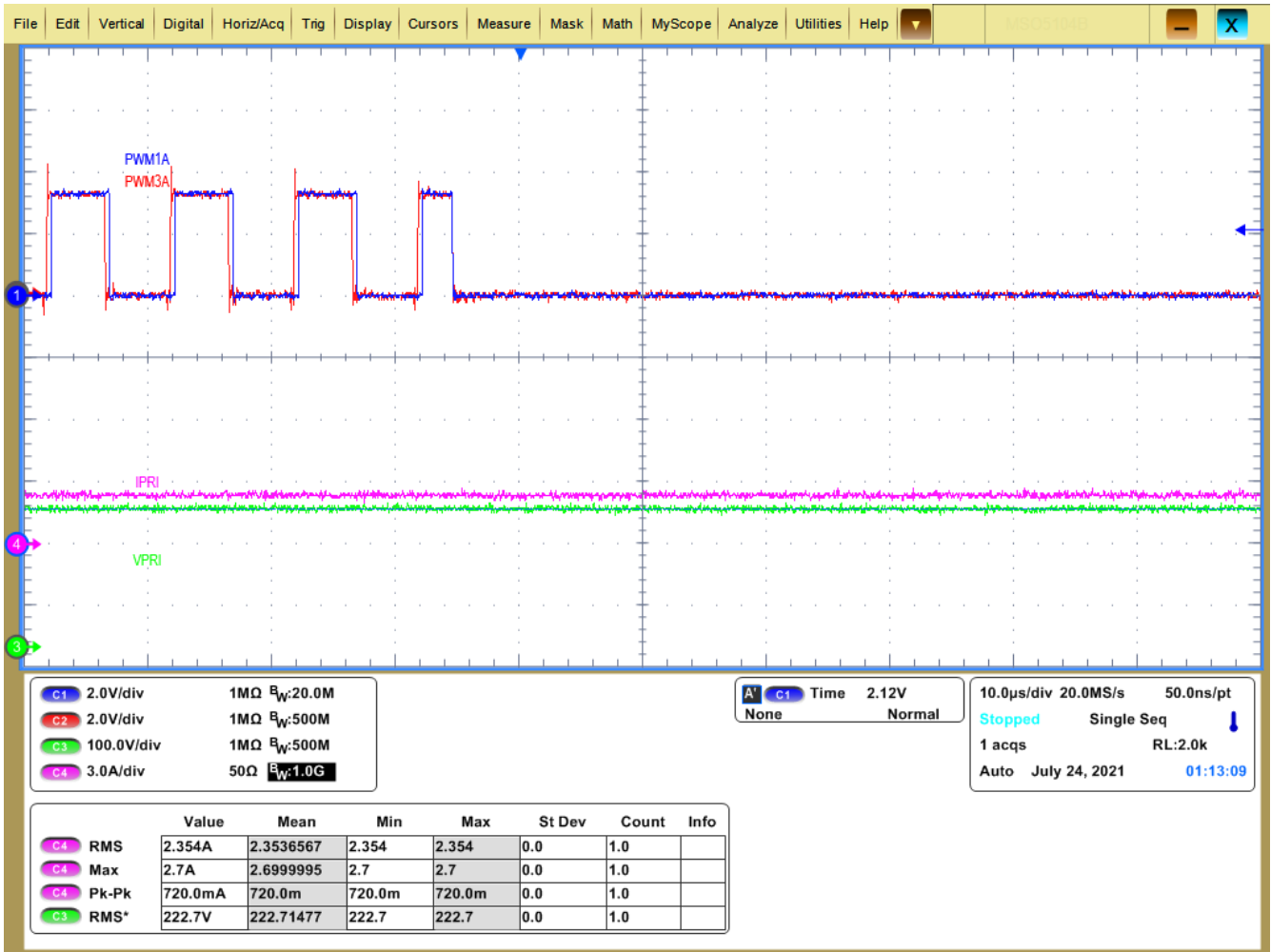
Figure 4-44. Lab 5 Reverse Power Flow Trip on Primary (Resistive Load), Limit Set = 2.5 A

4.5 Test Results

Testing and implementation of the DC/DC converter is carried out in two stages:

- Open-loop testing: In this phase, the PWM waveforms were configured at a fixed frequency of 100 kHz, and the phase between the input and output bridges were varied to get the desired output voltage and power levels. The performance of the converter is quantified by measuring the efficiency at different power levels.
- Closed-loop testing: In this phase, the converter is tested for its stability and its ability to track a reference voltage with good transient performance.

4.5.1 Open-Loop Performance

Table 4-4 shows the system efficiency as a function of output power. The converter output power was varied by changing the load and the phase angle between the input and output bridge to reach 10 kW. The table shows that the converter achieves a peak efficiency of 98.2% at approximately 6 kW and has a full load efficiency of 97.6% at 10 kW. Figure 4-45 shows the measured efficiency of the converter at different power levels.

Table 4-4. Converter Efficiency Results

TESTING CONDITIONS	INPUT VOLTAGE V_{IN}: 800 V, Switching frequency: 100 kHz, Phase shift: Between 10° to 15°, Load resistance: Decreased from 128 Ω to 34 Ω						INPUT VOLTAGE V_{IN}: 800 V, Switching frequency: 100 kHz, Load resistance: 26 Ω, Phase shift: Increased from 16° to 23°				
Load in Watts	500	1000	2000	3000	4000	5000	6000	7000	8000	9000	10000
Efficiency	91%	94%	97.50%	97.70%	97.90%	98%	98.16%	97.90%	97.80%	97.75%	97.60%
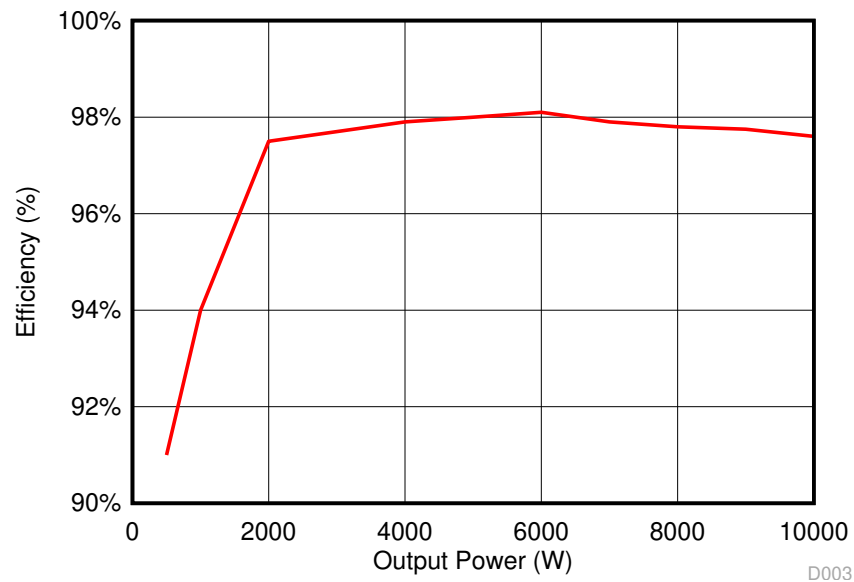
Figure 4-45. Efficiency Versus Output Power

Table 4-5 shows the resistive loads that were used to vary the output power from light load to full load. The input voltage is kept constant at 800 V. As seen from the table, to achieve power transfer of 10 kW, the phase angle is varied by keeping the load resistance fixed at 26 Ω. For a particular power output, input voltage, output voltage, switching frequency, turns ratio, and leakage inductance, the phase angle is calculated using Equation 14.

Table 4-5. Results Summary

INPUT CURRENT (A)	INPUT POWER (W)	OUTPUT CURRENT (A)	OUTPUT VOLTAGE (V)	OUTPUT POWER (W)	EFFICIENCY	LOAD RESISTANCE (Ω)	OBSERVED PHASE SHIFT (deg)	ACTUAL CALCULATED PHASE SHIFT (deg)
2.47	1976	3.875	496	1922	97.3%	128	10	7
4.37	3496	7.07	483.4	3416	97.7%	68	10	7
5.51	4408	9.06	473	4286	97.2%	52	10	8.5
7.79	6232	13.42	455.6	6114	98.1%	34	15	13
8.86	7088	16.49	419.4	6916	97.6%	26	16.2	16.32
11.56	9248	18.85	479.4	9036	97.7%	26	21.6	18.9
12.62	10096	19.68	500.5	9855	97.6%	26	23	20

Table 4-5 shows that the observed phase shift (calculated from the PWM settings) and the actual phase shift calculated from formula varies slightly. The theoretical formula gives a good starting point to set the phase shift, but depending on the load applied to the converter, there is a requirement for fine adjustment of phase to deliver the required power. At a phase shift of 23 degrees, full power transfer of 10 kW and an output voltage of 500 V for an input voltage of 800 V at a switching frequency of 100 kHz are obtained. The closed-loop regulation of output voltage to the desired value by controlling phase is being implemented and will be available following the release of this design.

Figure 4-46 shows the drain voltage (dark blue), gate voltage (cyan), and inductor current (purple) waveforms of the primary side SiC MOSFET at a 10-kW power level. The drain voltage switches between zero and 800 V, the gate voltage waveform switches from +15 / –4 V, and the inductor current has a trapezoidal signature with peak current of approximately 20 A.
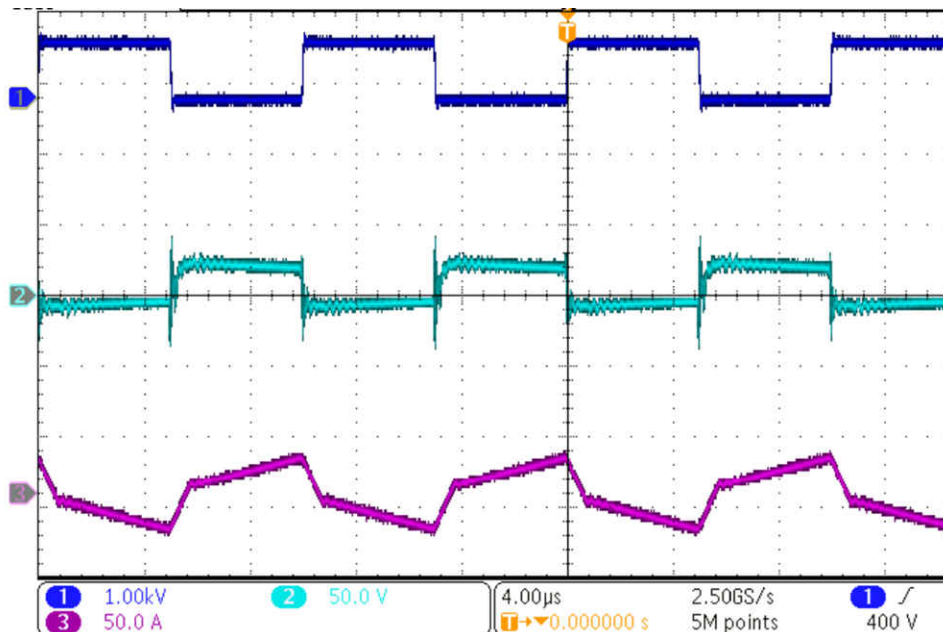

Figure 4-46. Waveforms at 10 kW

Figure 4-47 shows the waveforms at the instant of turn on. Gating pulses (dark blue) are applied to turn on the MOSFET once the drain voltage (cyan) falls to zero. This results in ZVS turn on of the MOSFET. Figure 4-48 shows the switch turn off waveform. The turn off process results in switching losses. This can be minimized by placing output capacitors across MOSFETs.
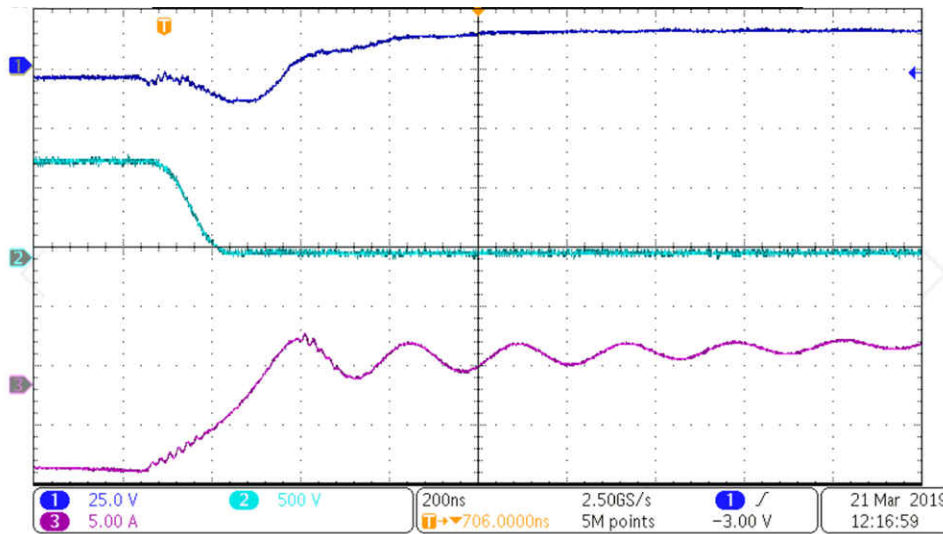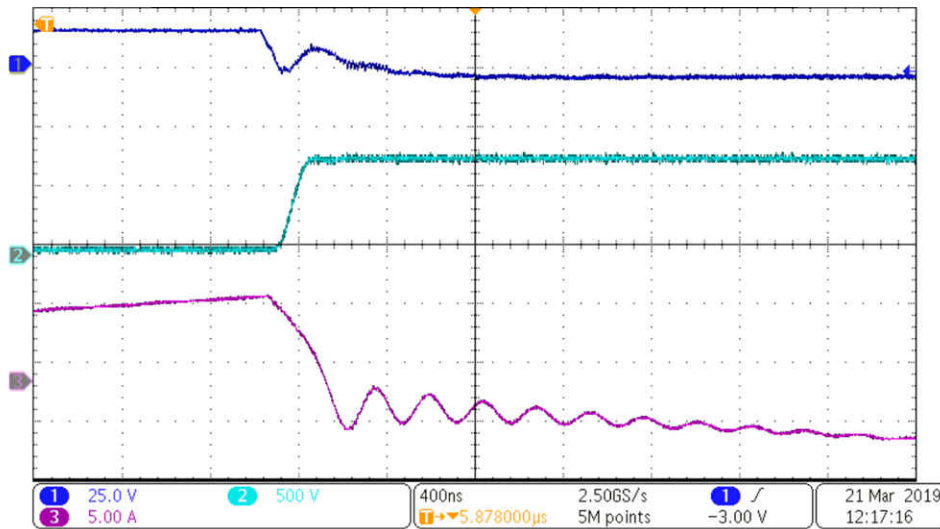

Figure 4-47. Switch Turn on Waveforms

Figure 4-48. Switch Turn Off Waveforms

Table 4-6 shows the dimensions of the converter. The calculated total power density of the converter is 2.32 kW/L, which is more than our targeted specification of 1 kW/L.

Table 4-6. Board Dimensions

AXIS	DIMENSIONS
X	328 mm
Y	160 mm
Z	82 mm
Volume	4.3 liter

4.5.2 Closed-Loop Performance

To quantify the closed-loop performance, the following functional blocks have been implemented in the current design:

- Sensing of primary and secondary voltages with the AMC1311
- Current sensing with the AMC3302 and AMC3306
- Temperature sensing with the TMP235 and LMT87 for addition possibility to protect power devices (not implemented in this design)

These functional blocks are interfaced with the F280049 MCU, where the signals can be processed to implement voltage mode or current mode control. Currently, digital control has not been implemented in this reference design. This section will be updated following the release of this reference design with test results on calibration of signal chain, stability, and closed-loop performance of the converter.

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-010054.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010054.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010054.

5.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010054.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010054.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010054.

6 Related Documentation

1. *Performance Characterization of a High-Power Dual Active Bridge dc-to-dc Converter*
2. *Performance of a 25kW 700V Galvanically Isolated Bidirectional DC-DC Converter Using 1.2kV Silicon Carbide MOSFETs and Schottky Diodes*
3. *Modeling and Optimization of Bidirectional Dual Active Bridge DC-DC Converter Topologies*

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7 Terminology

- SiC - Silicon Carbide
- DAB - Dual-Active Bridge
- ZVS - Zero Voltage Switching
- EV - Electric Vehicle
- CCS - Code Composer Studio
- V2G - Vehicle-to-Grid

8 About the Author

Harish Ramakrishnan is a Systems Engineer at Texas Instruments India, where he was responsible for developing reference design solutions for Grid Infrastructure sector. He received his Bachelor's degree in Electrical Engineering from NIT Durgapur, India and Master's degree from Texas A&M University, College Station.

N. Navaneeth Kumar is a systems engineer in C2000 group, Texas Instruments, where he is responsible for developing motor control solutions. N. Navaneeth brings to this role his extensive experience in power electronics, EMC, analog, and mixed signal designs. He has system-level product design experience in drives, solar inverters, UPS, and protection relays.

Manish Bhardwaj is a systems application engineer with C2000 Microcontrollers System Solutions Group at Texas Instruments, where he is responsible for developing reference design solutions for digital power, motor control, and solar power applications. Before joining TI in 2009, Manish received his Masters of Science in Electrical and Computer Engineering from Georgia Institute of Technology, Atlanta and his Bachelor of Engineering from Netaji Subhash Institute of Technology, University of Delhi, India.

Lei Song is a systems engineer at Texas Instruments Germany, where he is responsible for developing reference design solutions for Grid Infrastructure. Recently, he is focusing on system level reference design for EV Charging, Solar Energy and Energy Storage. Lei received his Master of Science in Electrical Power Engineering from Brandenburg University of Technology. In the past he has been working on IC developments for multi-rail PMICs, motor control MCUs, LED drives, magnetic current sensors and integrated AFEs.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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