Pseudo-Resonant Full Bridge DC/DC Converter

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***Abstract*—A new dc/dc converter topology is proposed which combines the ease of control and wide range of conventional dc/dc converters, with low switching losses, low dv/dt and low EMI that is typical of zero voltage switched resonant converters. Consequently, the ratings of these components are substantially lower than for similarly rated resonant topologies. Operation at very high frequencies is possible and is shown with the fabrication of a 200 W 1 MHz dc/dc converter.**

INTRODUCTION

THE "hard-switching" switched mode power supply continues to dominate the dc/dc converter arena in spite of the many problems that can be identified with it. The effort to obtain ever increasing power densities has been limited by the size of both the reactive elements and the isolation transformer. While component sizes tend to decrease with an increase in the switching frequency, device switching losses are proportional to frequency attainable in a given circuit. Even with the availability of extremely fast power MOSFET's, a frequency of 100 KHz seems to represent a typical maximum value. A switching frequency of 1 MHz is commonly considered the next significant milestone for power converters rated in the hundreds of watts. The higher frequencies are a key to realizing multiple benefits of higher power density and good transient response. The use of soft-switching techniques, as proposed in this paper, alleviates switching loss problems and allows a significant increase in the converter switching frequency. Further, as will be seen later, the proposed topology features device stresses comparable to ideal hard-switched PWM converters. This minimizes penalties typically associated with resonant and quasi-resonant converters, and makes the topology attractive for higher power applications.

Resonant mode dc/dc converters have long promised switching frequencies in the megahertz range, but with only limited success. The primary objective in selecting resonant mode operation has been the alleviation of device switching losses. Other advantages inherent in a resonant mode operation has been the alleviation of device switching losses. Other advantages inherent in a resonant scheme are well known and include low dv/dt or di/dt stresses, low EMI, and a good transient response. On the other hand, the choice of a resonant topology invokes substantial penalties in terms of higher VA ratings for the reactive elements and the devices. Further, as resonant converters transfer power through a variation of the LC circuit damping factor, they are also restricted in the load range, as represented by the fraction of the output V–I plane, that they can handle. Another constraint results from a use of the switching frequency as the control variable. Output control through frequency modulation requires that the magnetic components be rated for the entire range of operating frequencies. The variable switching frequency also makes suppression of conducted EMI difficult to implement. It is consequently not very surprising that resonant converters have not made major gains against conventional pwm dc/dc converters switching at 100 KHz.

This paper reexamines the basic premise behind resonant mode dc/dc converters. The ideal converter topology would combine the best features of resonant mode and pwm type dc/dc converters. This includes low switching losses, constant frequency operation, reasonably rated reactive components and a wide control and load range. A novel approach is proposed in this paper to allow zero voltage switching of all devices in a full bridge [13]. While resonant elements are used to ensure zero voltage switching of all devices, they have little or no role in the actual power transfer and can thus be reasonably sized. As the resonant elements are not involved in the primary power transfer, the converter is referred to as a pseudo-resonant converter. It will be seen that the new converter offers significantly higher levels of performance than either the PWM or typical resonant converters. Performance characteristics of resonant mode converters will be reviewed first.

Resonant Converter Topologies

A review of the literature shows that substantial effort has been put into developing resonant converter topologies for high frequency dc/dc power conversion. The thyristor based resonant converter as originally proposed by Schwarz and Klassens gave way to derivations of the circuit used with gate turn-off devices. The series and parallel output series resonant converters have been extensively discussed by various authors including Oruganti *et al.* [1] and Steigerwald [2], but the performance achievable was limited by snubber interactions and device nonidealities.

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A technique holding greater promise is the use of a zero current switching scheme for the alleviation of both device turn-on and turn-off losses [3], [4]. The scheme has been successfully implemented at low power levels in discontinuous mode "flyback" type dc/dc converters [5]. At higher power levels, the practical aspects of implementing a current zero switching scheme for very high frequency operation are extremely demanding. Parasitic inductances and capacitances and device (especially diode) recovery times, severely restrict the degree of control over the current zero point. This results in increased switching losses and often requires a snubber network of some kind, making operation in the megahertz range very difficult to attain.

It has been shown in previous papers [6]–[8] that zero voltage switching as opposed to zero current switching, is a more appropriate control strategy for high frequency resonant mode converters. Parasitic reactive elements in the converter reinforce the main resonant elements and yield substantial improvements in sensitivity performance. Diode recovery is no longer a problem and converter operation has been demonstrated at 1 MHz, even with slow 200-nS integral MOSFET rectifiers [6]. Incorporating the transformer magnetizing inductance as an element of the resonant circuit also makes it possible to handle loads ranging from open to short circuits. In spite of the substantial improvements realized through zero voltage switching, major problem areas can be identified. The entire output V–I plane is still not accessible. Further, resonant power transfer requires substantial penalties in terms of device and component ratings, while the use of frequency as the main control parameter makes magnetic components and EMI rejection circuits difficult to design.

An interesting departure from conventional resonant circuit topologies that has recently been proposed is the quasi-resonant converter of the resonant switch [9], [10]. Utilizing resonant components to shape the switching locus for the device, these topologies offer zero switching losses either through zero current or zero voltage switching. Further, power transfer does not occur via loading of the resonant components, a desirable attribute. Consequently, the dc characteristics are akin to conventional PWM type dc/dc converters, although duty cycle control is now obtained through frequency control. The use of the resonant switch has been extended to the various single transistor dc/dc converter topologies, such as the buck, boost and variations of the buck-boost topology. For converters requiring galavanic isolation, the resonant switch implementation of the flyback converter seems the only viable alternative. This indicates that for high power converters, multiple resonant switches are likely to be required. Interactions between the resonant elements of the various switches are likely to be extremely complex and will not result in a "clean" topology. The concept of a "resonant pole" as opposed to a resonant switch is presented next as a more viable building block for more complex high power dc/dc converters.

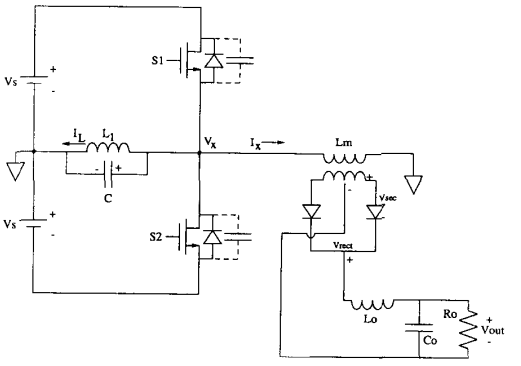

Fig. 1. Resonant pole circuit schematic.

Resonant Pole Operation

Fig. 1 shows a new approach to realizing zero voltage switching in resonant mode dc/dc converters. Two devices are configured in an inverter pole, with additional LC elements to provide zero voltage switching for both devices. Most typical zero voltage switching topologies are characterized by in-circuit voltage stresses which are substantially above the dc supply level. The proposed circuit features dc voltage levels which are clamped at the supply value. For the circuit to operate, switch $S1$ is maintained on until the current i_L is positive in the direction shown and equals a reference value I_p. Turning off $S1$ at this point requires that the current i_L now flow through the capacitor C. Sizing C correctly ensures that the voltage across the device $S1$ gradually increases in a resonant manner, thus ensuring zero voltage turn-off. Provided I_p was of sufficient magnitude, the voltage V_x "cosinusoidally" reverses and reaches the negative supply bus, at which point the diode $D2$, in antiparallel with $S2$, turns on and clamps the voltage V_x to $-V_s$. Now, $S2$ can be turned on at any time while $D2$ conducts without incurring any turn-on losses. $S2$ is maintained on until the current i_L reverses and equals $-I_p$, which initiates turnoff of $S2$. The cycle for $S1$ is similar and can then be repeated. Relevant waveforms are shown in Fig. 2. As in the case of the series resonant converter, the dc output can be either a series or parallel output.

Considering the parallel output case, as shown in Fig. 1, converter operation can be analyzed in two modes. Mode 1 is initiated at turnoff of $S1$. For the duration that V_x is greater than 0 V, the transformer primary current I_x equals the output current I_a. Under these conditions, the capacitor voltage, V_c, and the inductor current, i_L, are given by

$$V_c(t) = -(I_a + I_p)*Z_0 \sin \omega t + V_s \cos \omega t \quad (1)$$

$$i_L(t) = -(I_a + I_p) \cos \omega t + \frac{V_s}{Z_0} \sin \omega t - I_a. \quad (2)$$

As V_c passes 0 V, the rectifier current reverses direction and yields a new set of equations for V_c and i_L. These

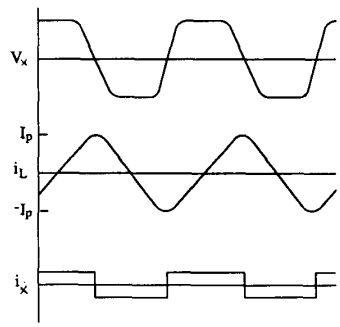

Fig. 2. Relevant waveforms for resonant pole circuit.

equations follow.

$$V_c(t) = -\left[\left(\frac{V_s^2}{Z_0^2} + (I_a + I_p)^2\right)^{1/2} - 2I_a\right] Z_0 \sin \omega t \quad (3)$$

$$i_L(t) = -\left[\left(\frac{V_s^2}{Z_0^2} + (I_a + I_p)^2\right)^{1/2} - 2I_a\right] \cos \omega t. \quad (4)$$

For proper operation of the resonant converter, it is necessary that V_c reach $-V_s$ in order to allow lossless turn-on of the incoming device, i.e., $S2$. Solving for this condition yields a limit on the value of I_p that is required for zero voltage switching

$$i_L(t) = -\left[\left(\frac{V_s^2}{Z_0^2} + (I_a + I_p)^2\right)^{1/2} - 2I_a\right] \cos \omega t. \quad (5)$$

Equation (5) indicates that, unlike in a typical resonant converter, I_p does not have to be substantially larger than I_a under rated power transfer conditions. Fig. 2 also shows that the rms current rating of the resonant capacitors is moderate, as current stresses are incurred only during the resonant transitions, and not when the devices are conducting.

The concept of the resonant pole allows zero voltage switching of multiple devices with moderately sized reactive elements and device stresses that are well contained. The resonant capacitor can be split and placed as shown in dotted lines in Fig. 1, so as to minimize the impact of system parasitic capacitances and inductances. While the topology of the resonant pole permits high frequency switching of the devices in the circuit, the control characteristics of the dc/dc converter leaves much to be desired. Under most operating conditions, the pole voltage V_x is essentially a square wave with cosinusoidal edges. Rectification and subsequent filtering yield a resultant dc voltage, which is rather weakly dependent on the switching frequency and load current. While the series output converter demonstrates better output control characteristics, it falls substantially short of the desired goals of accessing the entire output V–I plane. Noticing that the pole voltage is a square wave, and that the resonant pole corresponds to half a full bridge, it is proposed that a full bridge version of the resonant pole is likely to possess the desirable attributes. Such a topology is investigated next.

Full Bridge Pseudo-Resonant Converter

The pseudo-resonant converter proposed in this paper uses two resonant poles to realize the topology shown in Fig. 3 [13]. Control of this converter is similar to the phase shift control technique used in conventional hard switched full bridge dc/dc converters. In accordance with the operating principles of the resonant pole, incoming devices are turned on only when their drain-source voltage is zero. Furthermore, device turnoff is also accomplished with substantially 0 V across the device. The switching losses are therefore significantly reduced, ideally to zero, and the pseudo-resonant converter can operate at much higher frequencies than its hard switched counterpart.

Converter operation can be analyzed by independently observing switching transitions on the two resonant poles at the points denoted V_M and V_S. The switching transient at V_M is controlled by devices $S1$ and $S3$, while V_S is controlled by $S2$ and $S4$. Operation of devices $S2$ and $S4$ is synchronized to $S1$ and $S3$ through a controlled phase shift, represented by a time delay, t_2. Since V_S always lags V_M, the resonant pole containing $S1$ and $S3$ is referred to as the master phase while the devices $S2$ and $S4$ constitute the slave phase. Fig. 4 shows idealized waveforms of fV_M, V_S, inductor currents and the transformer primary voltage, V_{MS}, and current, I_{prim}.

With any of the switches $S1$–$S4$ conducting, the current in the corresponding inductor linearly changes so as to increase the current in the conducting device. Let us start analysis by assuming devices $S1$ and $S2$ to be conducting. On receiving a control command, device $S1$ is turned off. Unlike for the case of the resonant pole in Fig. 1, no mode change occurs as V_M crosses 0 V. It can be seen that I_{prim} continues to flow into the node over the duration of the entire switching transient, primarily because $S2$ is still conducting and the output rectifier ensures unidirectional power flow. Under these conditions the equations describing the behavior of V_M and I_{L1} are similar to (1) and (2) and are shown as follows:

$$V_M = -(I_p - I_{\text{prim}})Z_0 \sin \omega t + V_S \cos \omega t \quad (6)$$

$$i_{L1} = -(I_p - I_a) \cos \omega t + \frac{V_s}{Z_0} \sin \omega t. \quad (7)$$

Solving for the minimum current I_p needed to ensure a transition to the negative bus, it is found that zero voltage turn-on of the incoming device requires

$$I_p = I_{\text{prim}}. \quad (8)$$

Comparing (8) with the result in (5) it can be seen that the inductor current rating is lower than for the case of the resonant pole. Comparisons with conventional resonant topologies are even more striking.

Equations (6)–(8) assume zero losses in the resonant LC circuit. In actual practice, finite circuit losses hinder the transition of voltage V_M from one power rail to the other. In order to compensate for these losses, turnoff of $S1$ is initiated after the inductor current exceeds I_{prim} by an

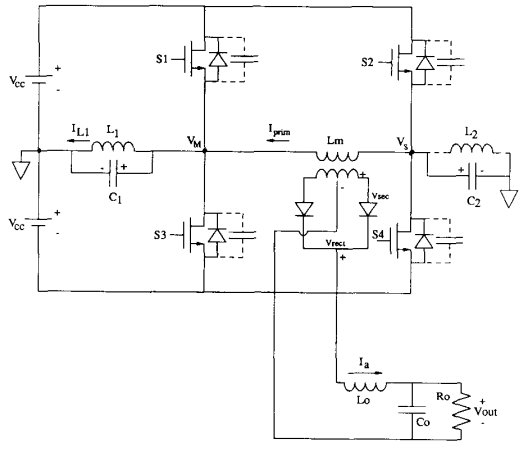

Fig. 3. Proposed pseudo-resonant dc/dc converter.

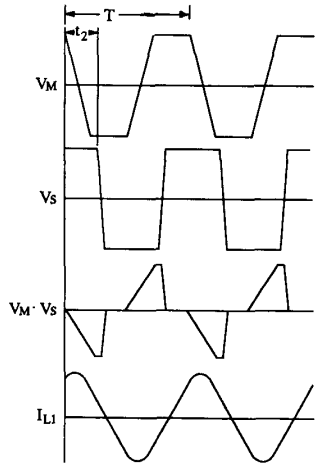

Fig. 4. Relevant waveforms for pseudo-resonant dc/dc converter.

amount that sufficiently compensates for the losses to be incurred during the switching transition. This is very similar to the priming of the dc link inductor that is typical of the resonant dc link inverter topology described elsewhere [11]. The losses that need to be supplied occur only in the resonant elements and are an insignificant, although important, fraction of the total power transferred.

Switching behavior on the slave side is significantly different from the master side in that the load current I_{prim} assists the inductor current i_{L2} in resonating V_S from one supply rail to another. This lack of symmetry in what seems to be a perfectly symmetrical topology has been commented on before and stems from the master/slave relationship enforced between the two phases [12]. The load current appears lagging in one phase and leading in the other. Consequently, the ratings for $L2$ and the devices $S2$ and $S4$ can be lower than for their counterparts in the master phase. In fact, if a reduction in the output V–I plane attainable is acceptable, it is possible to eliminate $L2$ entirely. This possibility is not discussed here in detail as a wide control range is one of the primary objectives for this topology [13].

Two alternate control strategies are seen to be possible for the pseudo-resonant converter. The first requires that the outgoing device, say $S1$, turn off when i_{L1} is a set fraction larger than the current I_{prim}. As per the analysis done previously, satisfying this condition ensures that the switching transition between supply rails is successfully completed. Alternately, turn-off of $S1$ may correspond to i_{L1} reaching a fixed value, I_p, which would then be slightly greater than the maximum load current to be handled. As the circulating currents in the first technique are substantially lower than with the second approach, higher converter efficiencies can be realized.

On the other hand, constraining the switching current level, I_p, to the maximum value, results in what is essentially as constant switching frequency mode of operation, with all the concomitant benefits. As a further simplification, the master phase can be excited by an external fixed frequency clock, with the slave phase operating synchronously, but with a controlled phase shift. This mode of operation sets up peak levels of I_p, which then become the maximum load current units for the resonant converter.

Design Considerations

While it is fairly clear that the choice of resonant elements is important, it is not very obvious how parameter selection should be done. Intuitively, it makes sense to minimize the values of L and C in each phase, as this results in the maximum switching frequency. However, the switching transitions between the two supply rails determine the extent of switching losses in the devices. An extremely fast transition could result in substantial losses, while slow transitions limit the maximum switching frequency attainable.

Further, the resonant capacitors only carry current during the transition and minimizing the ratio of transition time to the switching period significantly lowers the VA rating of these capacitors. On the other hand, an increase in the transition time results in substantial power transfer through the reactive components $L1$, $L2$, $C1$, and $C2$, an undesirable attribute. This dictates the choice of a transition time which is as small as possible within the constraint of low device switching losses.

With constant frequency excitation, the transition time for the master phase increases with load current reaching a maximum when $I_p = I_{\text{prim}}$. Under full load conditions, ignoring losses in the LC circuit, the transition time t_T can be calculated to be

$$t_T = \pi \sqrt{L_1 C_1}. \tag{9}$$

Under the same conditions, the time for which each device conducts, t_D is found to be

$$t_D = \frac{L_1 \cdot I_p}{V_B} \tag{10}$$

Thus, the switching period T is given by

$$T = 2\left(\pi\sqrt{L_1 C_1} + \frac{L_1 \cdot I_p}{V_B}\right). \tag{11}$$

Designing the converter for 1 MHz operation with a supply voltage $V_S = \pm 100$ V, with rated power output of approximately 200 W. The transition time t_T at full load is to be constrained to 200 nS. Considering the waveform across the rectifier, this gives a peak value of approximately 4 A for I_p.

Calculating the values for $L1$ and $C1$ yields

$$L_1 = \frac{V_B}{I_p}\left(\frac{T}{2} - t_T\right) = 7.5\ \mu\text{H} \tag{12}$$

$$C_1 = \frac{I_p}{V_B \pi^2} \cdot \frac{t_\mu^2}{\left(\frac{T}{2} - t_T\right)} = 550\ \text{pf}. \tag{13}$$

Designing for the values of $L2$ and $C2$ follows similar lines of reasoning. It is important to note that for the slave phase, the slowest transition occurs at no load and the fastest transition at full load. Constraining the slowest transition to 200 nS as before, values for $L2$ and $C2$ can similarly be found. Values of $L2$ and $C2$ used are $L2$ = 12 μH, $C2$ = 550 pf.

These component values are used to simulate converter performance using Advanced Computer Simulation Language (ACSL). The transformer is assumed to have a large magnetizing inductance as well as a leakage reactance X_{1i}.

Fig. 5 shows typical waveforms obtained during the simulation. Fig. 5(a) shows the master and slave phase voltages corresponding to a load of 7.5 Ω and a phase delay t_2 − 200 nS. Fig. 5(b) shows corresponding values for i_{L1} and i_{L2}. Fig. 6 depicts the transformer primary voltage and current under the same conditions. Fig. 7 shows the relationship between i_{L1} and I_{prim} for a 1-Ω load. An output V–I plane plot is compiled from successive computer runs and is shown in Fig. 8. The output voltage is seen to decrease with an increase in load current. Two major contributing factors for this group are the transformer leakage reactance and variations in the transition time t_{tr}, with load current. The droop can be modeled as the effect of a thevenin resistance, R_{TH} [13]. To find R_{TH}, the droop in voltage ΔV_0 versus I_0 shows a virtually linear relationship, from which R_{TH} is estimated to be 0.92 Ω.

Experimental Verification

A prototype pseudo-resonant dc/dc converter was fabricated in the laboratory. When operated from a ±100-V dc supply, the converter delivered 175 W at 1 MHz. Commercially available MOSFET's (IRF 352) were used to realize the switches. As anticipated, circuit layout was critical and identification of the dominant stray inductances and capacitances in the circuit was of primary importance. To take advantage of the topology, the resonant capacitors $C1$ and $C2$ were split in half and placed directly

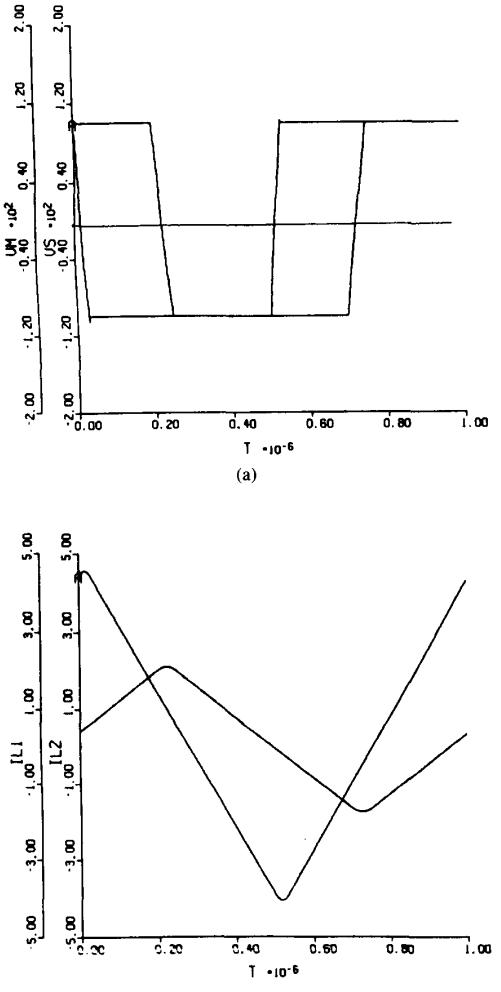

Fig. 5. Simulated waveforms for (a) V_M and V_S for R_0 = 7.5 Ω, I_a = 2.25 A, V_0 = 16.8 V, t_2 = 200 nS, (b) I_{L1} and I_{L2} for the same conditions.

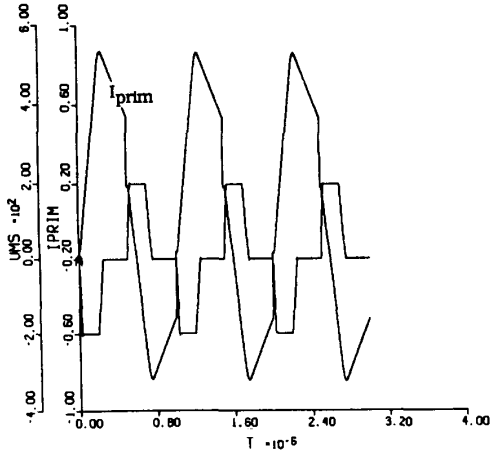

Fig. 6. Simulated waveforms showing transformer primary voltage V_{MS} and primary current I_{prim}. Same conditions as Fig. 5.

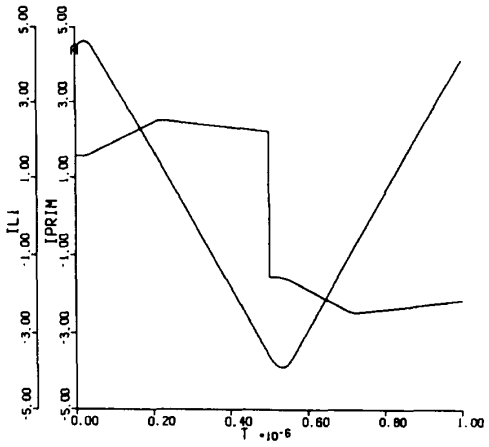

Fig. 7. Simulated waveforms showing I_{prim} and I_{L1} for R_0 = 1 Ω, I_a: 9.6 A, V_0 = 9.6 V, t_2 = 200 nS.

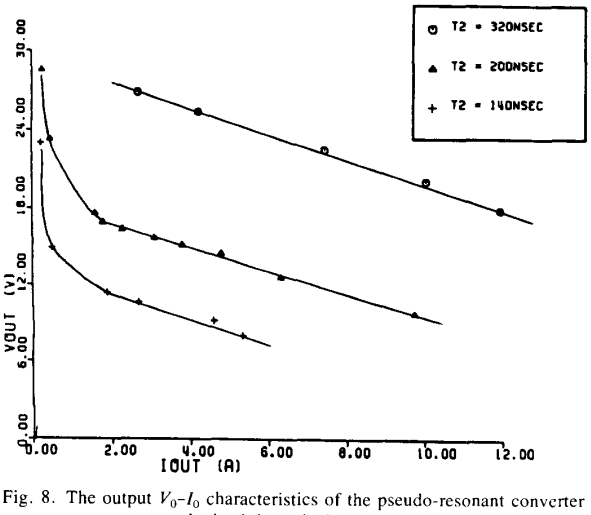

Fig. 8. The output V_0–I_0 characteristics of the pseudo-resonant converter obtained through simulation.

across the drain to source terminals of each device. This equivalent orientation ensures that $L1$ and $L2$ are in series with equivalent series inductance of the filter capacitor and the connecting leads. In addition the 200 pf drain-source capacitance of each device is in parallel with the capacitance $C1$ (or $C2$). This ensures minimum stray inductance in the critical path connecting the device to its resonant capacitor.

Efforts to optimize the design of the magnetic components was stymied by the non-availability of ferrite cores for high power applications in the megahertz frequency region. Evaluation of various core materials was performed at 0.5–2 MHz using a test fixture that allowed us to calculate the values of inductor ESR and an equivalent core loss resistor, R_p, represented in parallel with the inductor being tested. Ferroxcube 4C4 core material was seen to be substantially superior to other materials including 7C4 and 3C8 materials. However, 4C4 material is aimed at low power pulse transformer type applications and has a very limited selection of pot cores and toroids available. This proved to be one of the major limitations of our design process.

While we would have preferred to operate the transformer at 0.06 T or less to avoid excessive core losses, we were forced to design around 0.1 T because of limitations in pot core sizes. Copper losses in the transformer and inductor were minimized using 18-gauge Litz wire. The final values of all the reactive components follow

$$L1 = 6\ \mu\text{H},\quad L2 = 12\ \mu\text{H},\quad C1/2 = C2/2 = 100\ \text{pf}$$

$$L_m = 60\ \mu\text{H},\quad L_{l1} = 2.2\ \mu\text{H},\quad C_f = 1700\ \mu\text{f}$$

$$L_0 = 3\ \mu\text{H},\quad C_0 = 2200\ \mu\text{f}$$

where L_m and L_{l1} are the transformer magnetizing and leakage inductances measured from the primary side, and C_f is the filter capacitor supporting the ±100-V dc bus.

The gate drive circuit proved to be a critical part of system design as well. The problems essentially stemmed from providing a voltage sensing feature, which enabled the gate drive only when the device voltage approached 0 V. Incorporating this sensing feature into the main controller proved extremely difficult, given the propagation delays that would have been acceptable. Consequently, voltage sensing for turn-on was added to individual gate drivers. The turn-off signal, on the other hand, was directly initiated from the main controller.

The converter operated as expected and provided substantial reduction in the device switching losses. Although we constrained operation to 1 MHz, there appears to be no reason why the converter section could not be operated at higher frequencies. Fig. 9 shows typical converter waveforms at approximately 100-W output. Fig. 9(a) shows V_M and V_S with a time delay of 200 ns between the phases. Fig. 9(b) shows the current i_{L1} and the transformer primary current I_{prim} for the same load, while Fig. 9(c) shows the voltage impressed across the output filter.

Reverse recovery of the output rectifiers resulted in large voltages spikes on the transformer secondary as can be seen in Fig. 9(c). This problem is inevitable in transformer coupled inductive filter circuits. Energy stored in the transformer leakage inductance at the instant of diode snap-off has to be handled, often dissipatively. A purely capacitive output filter stage would substantially reduce the problem, but would now require output capacitors with very large ripple current ratings. The voltage spike was contained with a capacitive voltage clamp. Energy stored in the clamp circuit was then partially returned to the output capacitor. Problems at the rectifier interface can be reduced through a minimization of the transformer leakage inductance and the use of fast, soft recovery diodes.

In terms of control characteristics, the pseudo-resonant converter fulfilled expectations and gave control over the entire output V–I plane to within its maximum power rating. Fig. 10 shows the V–I control characteristics for three typical delay times. The Thevenin resistance R_{RH} is seen

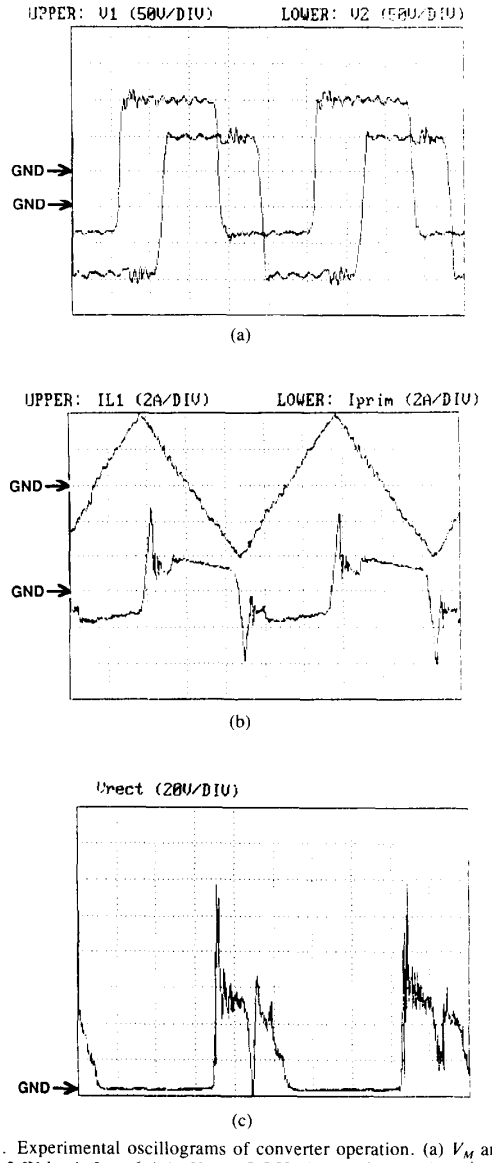

Fig. 9. Experimental oscillograms of converter operation. (a) V_M and V_S for 99.2-W-load, I_0 = 6.4 A, V_0 = 15.5 V, time scale = 200 nS/div. (b) I_{L1} and I_{prim} form same conditions. (c) V_{rect} form same conditions.

to vary from 0.6 to 0.85 Ω. This variation is a result of droop in the dc bus voltage with increase in the output power.

The efficiency of the converter constructed in the laboratory was measured at 72.8% from ac input to dc output under full load conditions. This corresponds to 63 W losses at 135 W output power. Losses measured at no load were 23.4 W. The poor efficiency resulted from two main sources of dissipation. Losses due to transformer leakage inductance were estimated at 23 W while voltage sensor losses were 5.5 W. Losses in the MOSFET's were approximately 2.1 W per device at full load, demonstrating the successful application of zero voltage switching.

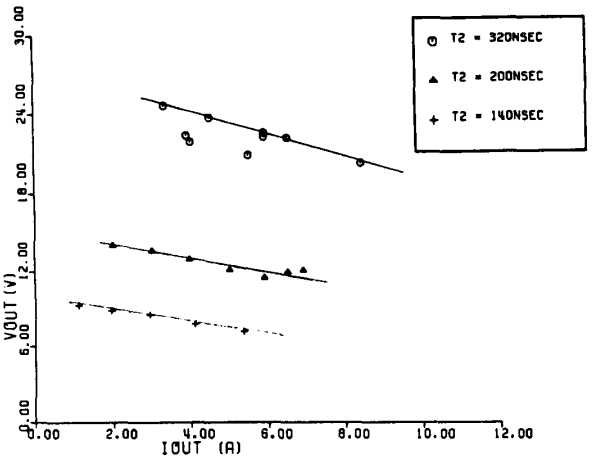

Fig. 10. Experimentally obtained V_0-I_0 plane form the pseudo-resonant converter.

Conclusion

The increasing importance of resonant mode dc/dc converters for high frequency applications is reexamined in this paper. It is seen that most resonant topologies extract substantial penalties in terms of component and device *VA* ratings, while significantly limiting the control range attainable by the converter. Quasi-resonant converters built around the concept of the resonant switch are an interesting alternative, but are not suitable for higher power levels.

The concept of a resonant pole has been proposed in this paper. Building on the operating characteristics of the resonant pole, a full bridge pseudo-resonant dc/dc converter has been realized and is shown to possess extremely desirable attributes. These include:

- reasonable component and device ratings;
- minimal switching losses with zero voltage switching;
- wide control range;
- 1-MHz operation at 200 W;
- simple control;
- insensitive to circuit parasitics;
- low dy/dt stresses;
- constant frequency operation;
- moderate di/dt stresses.

The converter was fabricated and tested at 200 W at a switching frequency of 1-MHz.

Acknowledgment

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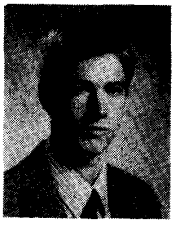

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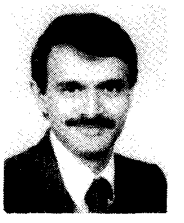

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