覆铜高级连接方式

如过孔全连接,焊盘热焊盘连接;顶层 GND 网络全连接,其他层热焊盘连接线宽 0.3mm

在 AD PCB 环境下, Design>Rules>Plane> Polygon Connect style,点中 Polygon Connect style,右键点击 new rule ------新建一个规则 点击新建的规则既选中该规则,在 name 框中改变里面的内容即可修改该规则的名称,默认是 PolygonConnect_1,现我们修改为 GND-Via,选项 Where The Frist Object Matches 选Advanced (Query), Full Query 输入IsVia (大小写随意), Connect Style 选 Direct Connect, 其他默认设置,点击下边的priorities 把GND-Via规则优先级置最高,(1为最高,2次之...)如下图:

🖃 😼 Design Rules		Name	
🛨 장 Electrical		PolygonConnect	Name GND-Via Comment
主 🍣 Routing			
😟 🖦 SMT			Where The First Object Matches
📺 💷 Mask			
🖻 😳 Plane			
😑 😳 Power Plane Connec	t Style		
😳 PlaneConnect			Vinet Class
🖃 😳 Power Plane Clearand	ce		O Layer Ouery Helper
😳 PlaneClearance			Net and Layer
🖃 😂 Polygon Connect Styl	e		Advanced (Query) Query Builder
😳 PolygonConnect	<u>N</u> ew Rule		
🗄 💇 Testpoint	<u>D</u> elete Rule.		Where The Second Object Matches Full Query
🗄 ᅏ Manufacturing			
🕀 🚟 High Speed	<u>R</u> eport		O Net
🛨 🚺 Placement	R		🔘 Net Class
🗄 🍿 Signal Integrity	<u>Export Aules</u>		Layer
	<u>I</u> mport Kules		Query Helper
			Constraints
			Connect Style
			Direct Connect 🖌
Priority Enabled Name	Scope	Attributes	
1 🗹 GND-Via	IsVia	All Style - Direct Co	nnect
2 🔽 PolygonCor	onect All -	All Stule - Belief Cor	nnect Width = 10mil Angle = 90

回到 PCB 设计环境下进行覆铜,覆铜网络选 GND,覆好铜以后对于网络为 GND 的 Via(过孔)将为全覆铜的连接,而非默认的 relief connect 方 式(热焊盘方式),由于规则是对过孔的全连接覆铜,所以对于焊盘的覆铜是热焊盘方式连接方式,见下图(左):





如果想过孔和焊盘多用热焊盘方式,那在 Full Query 修改为 IsVia or Is pad ,更新下刚才的覆铜,地焊盘也全连接了,如上图(右)同样也 可 以 Full Query 为 Is pad , InNet('GND') , InNet('GND') And OnLayer('TopLayer'), InComponent('

U1'),InComponent('U1') OR InComponent('U2') OR InComponent('U3') , innetclass('Power')等等...

1.InNet('GND') 对于网络名为 GND 的网络进行覆铜连接,覆铜连接规则采用 InNet('GND')的覆铜连接规则,注: InNet('X'),X 为 PCB 中的网络名, Connect Style 可 全连接 或 热焊盘 或 无连接 方式; 热焊盘方式还可设置 2,4 连接,45 度,90 度和连接线宽,下面 的也类同;

2.InNet('GND') And OnLayer('TopLayer'),对于位于 TopLayer 层的 GND 网络进行的覆铜采用该覆铜连接规则,OnLayer('X'),X 为层名,层名称修改可通过 Design>Layer Stack Manager,双击层名称修改。;

3.InComponent('U1'),对于元件U1的覆铜采用该覆铜连接规则,U1上有个 X 网络,同时覆铜的网络也为 X,这样改规则才有效果,例 如U1上有个管脚连接到 GND 网络,同时覆铜网络选 GND,此时改规则才有效果;否则等于没有这个规则,与不建立规则效果一样;

4.InComponent('U1')OR InComponent('U2')OR InComponent('U3')对于 元件 U1,U2,U3 采用该覆铜连接规则,即 U1,U2,U3

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多采用改覆铜连接规则,关系是 OR ,而非 AND;

innetclass('Power'), Power 类网络的覆铜连接方式规则, Design>Classes 创建一个规则类, 类的方式有多种, 网络类, 元件类, 层类等。

网络类指向 PCB 中的网络名, 层类指向 PCB 中的元件(焊位), 层类指向 PCB 中的层;;; 例: innetclass('Power'), 在 net classes (网络类)下新建一个规则(new rule),同样是右键增加,并改名为 Power,选中这个网络类规,添加左边的的网络到右边去,比如添加 GND, VCCINT,

VCC3.3, VCC1.2, VCCA, GNDA 等...这样在多个多个网络的不同覆铜就不用分别建立 GND , VCCINT , VCC3.3 , VCC1.2 , VCCA , GNDA 的 覆铜连接规则, 自需要建立一个网络类覆铜连接规则即可, 在覆铜的时候覆铜网络连接到相应的网络即可;

注意:所有上面的规则多要设置相应的优先级和新建规则,新建规则的优先级设为高,默认规则的优先级最低,其他优先级看实际排列。所有选项选Where The Frist Object Matches选Advanced (Query),Full Query 输入相应的数据命令,对于相对简单的类似只是网络和层的覆铜连接InNet('GND') And OnLayer('TopLayer')---项层地网络的覆铜连接方式,可选择The Frist Object Matches---Net and Layer,在里面的下拉框中选择相应的Net和Layer后。Full Query框软件会执行填充数据,完成后ApplyOK回到PCB中(Full Query框中语法错误,软件会提示错误,而填入一个不存在的层或网络名则不会),再在PCB进行覆铜选择相应的覆铜网络即可,覆铜间距默认是10mil,如需特殊间距则需修改间距规则;

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高级间距规则

比如覆铜间距 <mark>16mil,其他安全间距</mark> <mark>8mil,过孔到过孔间距</mark> 100mil,焊盘到焊盘间距 100mil,焊盘到过孔间距 100mil,顶层地覆铜 0.8mm,顶层 VCC3.3 与 VCC1.8 覆铜间距 0.5mm 等

Altium Designer 的间距规则默认为一个 10mil 间距,没有区分焊盘到焊盘,过孔到过孔,走线到覆铜等的间距,想要高级规则,必须自己新建。

在 PCB 设计环境下 Design>Rules>Electrical>Clearance,同样右键新建一个间距规则并重命名为 Poly,Where The First Object Matches 选 Adcanced (Query),Full Query 输入 inpolygon, Constraints 把默认的 10mil 修改为 20mil,优先级 Poly 比默认的的 Clearance 的 10mil 高,这 2 个间距规则共同构成覆铜间距为 20mil,其他间距例如走线到走线,走线到焊盘过孔间距为 10mil 的规则,如下图:

Design Rules Electrical Clearance Clearan	<u>New Rule</u> Delete Rule <u>R</u> eport <u>E</u> xport Rules. <u>I</u> mport Rules.	· · ·	Name Poly Where The First Obje All Net Net Class Layer Net and Layer Advanced (Query Where The Second C All Net Net Class Layer Net Class Layer Advanced (Query Net Class Layer All All All All All Advanced (Query All Advanced (Query Advanced (Query	ect Matches Query Help Query Build Define the s Query Help Query Help Query Help Query Help Query Help Define the s Def	Comment	Full Query inpolygon Full Query All
			Constraints			
Edit Rule Prio Rule Type: Clearan Priority Enabled 1	orities ce Name Poly	Scope inpolygon - /	Attributes	Differe	ent Nets Only Minimum Cle	arance 20mil
2 🗹 (Clearance	All - All	Clearance = 10n	nil	C	

下 2 图是过孔覆铜全连接 viaconnect, 默认安全间距 clearance 8mil, 覆铜间距 16mil 规则的覆铜, inpolygon 是所有的覆铜, 如果想要其他覆铜间距,则需要在新建覆铜规则,比如 VCC3.3 覆铜 0.5mm, VCC1.8 覆铜间距 0.6mm,其他覆铜 0.4mm;优先级 16mil 的最低;覆一片铜到 VCC3.3 网络同时起名该覆铜为 VCC1.8-ALL;同样要兴建间距规则,见下面第 3-6 张图:

	Design Rules Electrical Clearance Poly Clearance	Name Poly Where The First Object Matches Full Query
	Name viaconnect Comment Where The First Object Matches Full Query All isvia	 All inpolygon Net Net Class Layer Query Helper Advanced (Query) Query Builder
□ Tun-Routed Net		Where The Second Object Matches







Net and Layer

Different	Nets	Only	
	-	01	



O Advanced (Query)	Query Builder	
Constraints		



1	dit Ru	le Pri	iorities		?	×
	<u>R</u> ule Type	: Cleara	nce			1
	Priority	Enabled	Name	Scope	Attributes	
	1	~	VCC1.8-ALL	InNamedPolygon (VC	Clearance = 0.6mm	
	2	~	VCC3.3-ALL	InNamedPolygon (VC	Clearance = 0.5mm	
	3	✓	OtherPoly	inpolygon - All	Clearance = 0.4mm	
	4	✓	Clearance	All - All	Clearance = 0.254mm	

Increase Priority	Close

下图是过孔到过孔的间距规则, Where The First Object Matches, Where The Second Object Matches 的 FullQuery,只有这 2 个参数一个是 isvia, 另一个是 ispad 即可;如果一个是 ispad 另一个是 isvia,那就是过孔到焊盘的间距;如果一个是 ispad 另一个是 ispad,那就是焊盘到焊盘的间距; 随后填入具体的间距即可,Where The Second Object Matches 默认是 ALL,修改他就是第一个和第二个间距规则, IsVia 和 ALL 就是 Via 到其 他的间距规则, IsVia 和 IsVia 就是过孔到过孔的间距规则;



注:设置小间距管脚间距:一些FPGA芯片等很多焊盘间距多达到了0.2mm,默认的10mil(0.254mm)间距显然是冲突的,上述问题可以通过 HasFootprint('PQ208')或IsPad **and** InComponent('U1');(IsPad **and** InComponent('JP4'))**or**(IsPad **and** InComponent('JP3')) HasFootprint('PQ208'),封装为 PQ208 的元件; sPad **and** InComponent('U1'),元件 U1 的管脚间的间距;

上面 2 个规则只是管脚间距,丛上面拉出来的线的间距是其他的规则值,当然不能太大;比如上面的 PQ208 焊盘 0.3mm。焊盘间距 0.2mm,布线 0.2mm,那拉出来的线间距就是 0.4mm。如果把布线间距设为 0.5mm,1mm ,要么绿色,要么拉不出来; (IsPad **and** InComponent('JP4')) **or**(IsPad **and** InComponent('JP3')),元件 JP3, JP4 的间距规则; 见下面 3 张图:







Name	Clearance		Comment [Unique ID HPXAKJTN	И
Where All All Net Laye Adv	The First Obje Class er and Layer anced (Query)	ct Matches Query Help Query Build	er	Full Query (IsPad (IsPad (IsPad (IsPad (IsPad	and and and and and	<pre>InComponent('JP4')) InComponent('JP3')) InComponent('u2')) InComponent('jp5')) InComponent('jp2'))</pre>	or or or or
Where All	The Second O	bject Matches	~	Full Query All			

下图是一个定位孔间距为 3mm 的间距规则:常用一个内孔=外孔的焊盘做定位孔。该孔不连接到任何网络(不进行电气连接),只拧螺丝用 我们在 PCB 上 4 个脚上放 4 个定位孔,不连接到任何网络,焊盘名称起为 HOLE,内孔=外孔大小; free-hole 含义 free 不连接到任何网络, Hole 焊盘名称;可以是 free-0, free-1, free-2 等等;

Design Rules Electrical Clearance visto-vis	Name pholeClearance Comment	Uni
PholeClearance	Where The First Object Matches All Net Net Class Layer Net and Layer Advanced (Query)	Full Query HasPad('free-HOLE')
7	Where The Second Object Matches All Net Net Class Query Helper Constraints	Full Query
	Different Nets Only	earance 100mil

下图为一个在 toplayer 层覆铜名为 5VANA 的间距规则,当然 toplayer 可以换成其他层,5VANA 可以换成其他覆铜的名称;

🖃 🕶 Design Rules	
Electrical	Name top_5VANA Comment Unique ID LD
Clearance top_5VANA VCC1.8-ALL VCC3.3-ALL OtherPoly Clearance Short-Circuit ShortCircuit	Where The First Object Matches Full Query All InNamedPolygon ('5VANA') Net Query Helper Net and Layer Query Helper
UnRoutedNet Un-Connected Pin Routing SMT Mask Plane Power Plane Connect Style PlaneConnect Plane Clearance	 Advanced (Query) Query Builder Where The Second Object Matches All Net Net Class Layer Query Helper Net and Layer Query Builder
PlaneClearance Polygon Connect Style PolygonConnect PolygonConnect Manufacturing High Speed Placement	Constraints Different Nets Only Minimum Clearance 0,4mm



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下图为 DM 到 DP 网络间距为 20mil 的间距规则:



Different Nets Only Minimum Clearance 16mil

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高级线宽规则

Tinteractive Routing For Net [G	ND] [mil]	? 🗙
Properties Vi. 12 Width from rule preferred value Image:	a Hole Size 2mil Via Diameter 22mil ayer TopLayer 💽	Bouting Conflict Resolution None Push Conflicting Object Walkaround Conflicting Object Hug And Push Conflicting Object Interactive Routing Options Interactive Routing Options Restrict To 90/45 Auto Complete Automatically Terminate Routing Automatically Remove Loops Hug Existing Traces (Walkaround Mode)
Via Style Constraints Edit ⊻ia Rule Via style is currently constrain maximum hole sizes are 0mil a 0mil and 24mil.	and 14mil. The minimum and maximum diameters are	Smart Connection Pad Exits ✓ Allow Diagonal Interactive Bouting Width / Via Size Sources ✓ Pickup Track Width From Existing Routes Vrack Width Mode Via Size Mode Rule Preferred ✓ Eavorite Interactive Routing Widths Favorite Interactive Routing Via Sizes
Menu		OK Cancel
Design Rules Electrical Routing Width WGND Width Routing Topology Routing Topology Routing Priority Routing Priority Routing Layers Routing Corners Routing Corners Routing Via Style Routing Via Style Fanout Control Differential Pairs Routing DiffPairs Routing	Name W_VCC Where The First Object Matches All Net Net Class Layer Net and Layer Advanced (Query) Query Builder Constraints Preferred Width Omil Min Width 10mil Max Width Omil	Ent Full Query InNet ('VCC') Characteristic Impeda

设置 GND 网络 30mil, VCC 网络线宽 20mil, 布线时按 TAB, Track Width Mode 选 Rule Preferred;



	Ť	†	🔽 Layers in la	ayerstack o
Attributes on Lay	er		Layer Stack Refere	nce
Min Width	Preferred Size	Max Width	Name	I /
10mil	20mil	100mi	TopLayer	0
10mil	20mil	100mil	BottomLayer	1



Edit Rule Priorities 🔹 🤶 🔀				
Rule Type: Width				
Priority	Enabled	Name	Scope	Attributes
1	✓	W_VCC	InNet(VCC')	Pref Width = 10mil Min Width = 10mil Max Width = 100mil
2	✓	WGND	InNet('GND')	Pref Width = 10mil Min Width = 10mil Max Width = 100mil
3	✓	Width	All	Pref Width = 8mil Min Width = 8mil Max Width = 30mil





另外还可以添加类来设置线宽规则,适合大批量线宽处理;

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