电平转换原理和使用

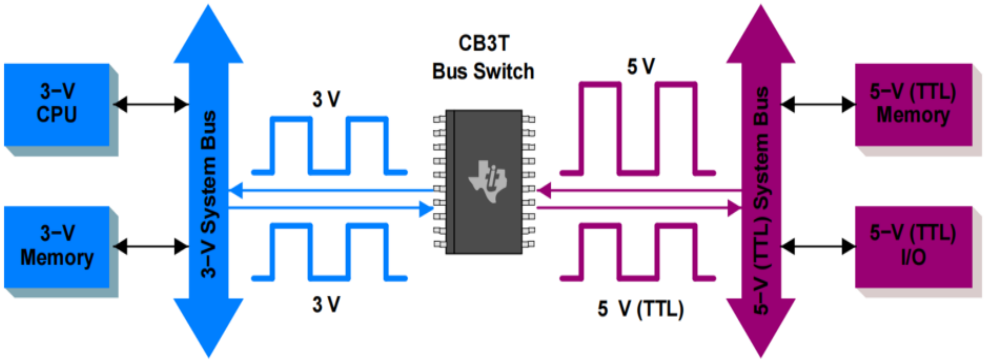
主讲人：大话硬件

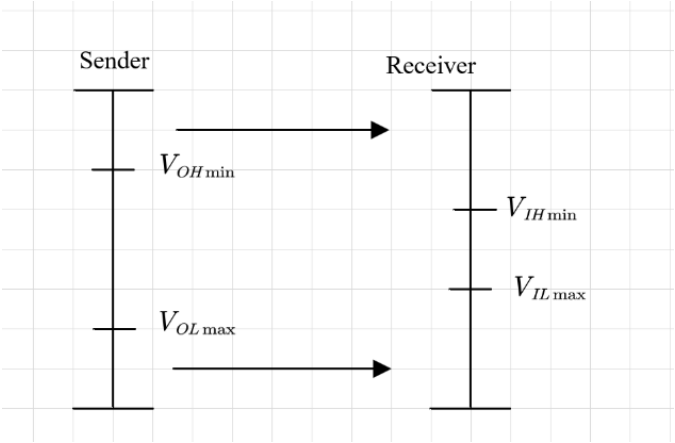
目录

电平转换使用背景

背景

两个器件正常通信需要满足电平要求标准，否则无法准确识别





电平转换分类

电平转换电平类型

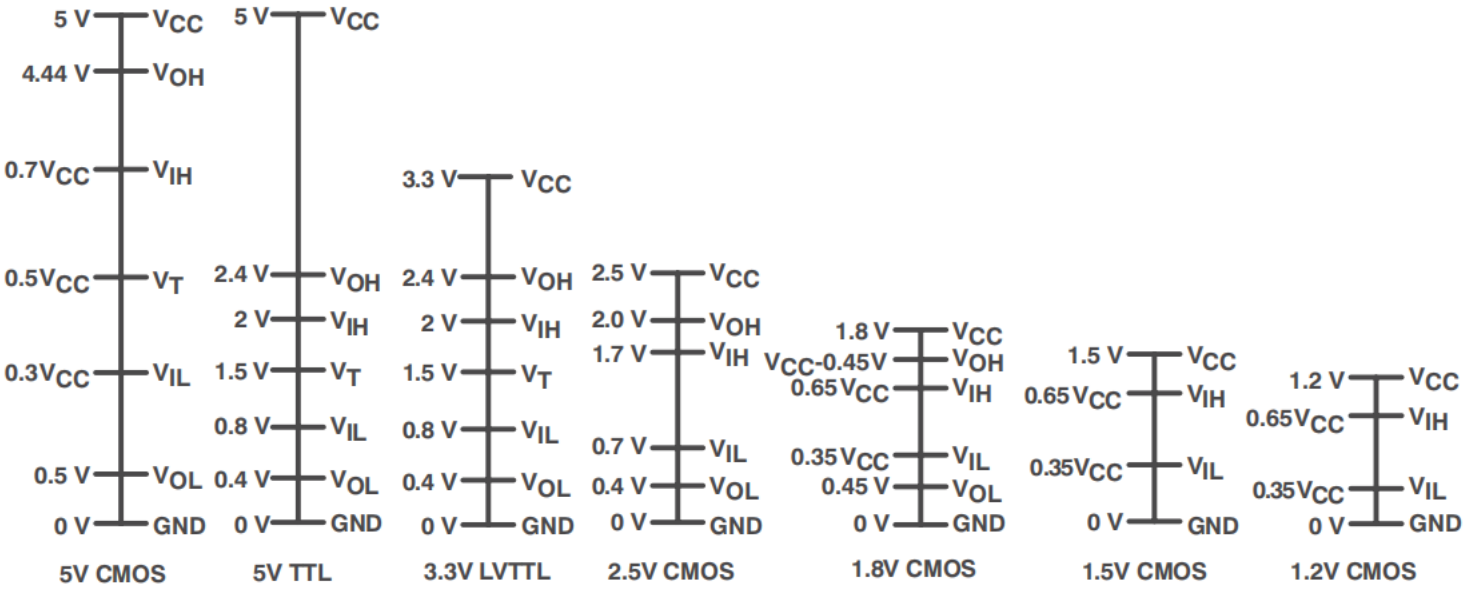
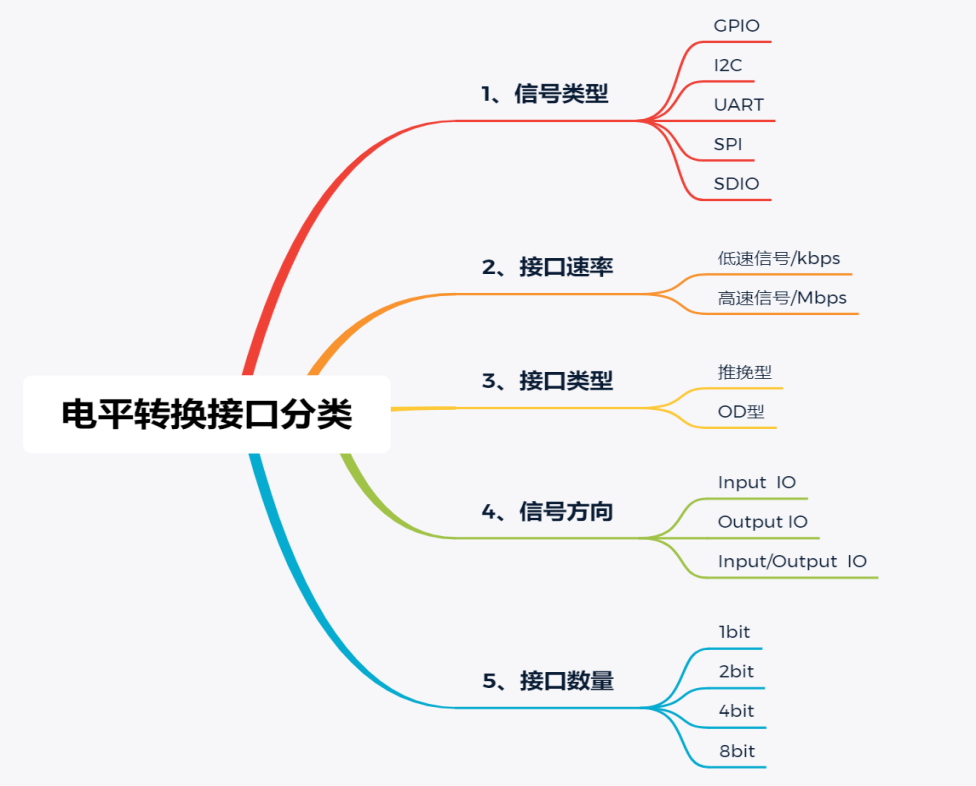


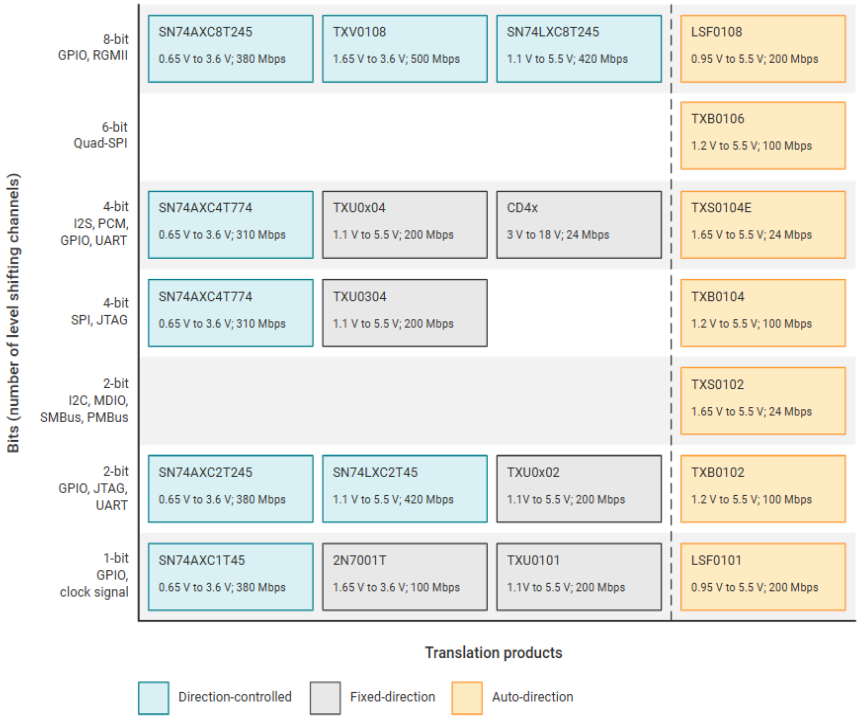
Figure 1. Digital Switching Levels

电平转换接口分类



电平转换分类

电平转换芯片分类



Overview of device families

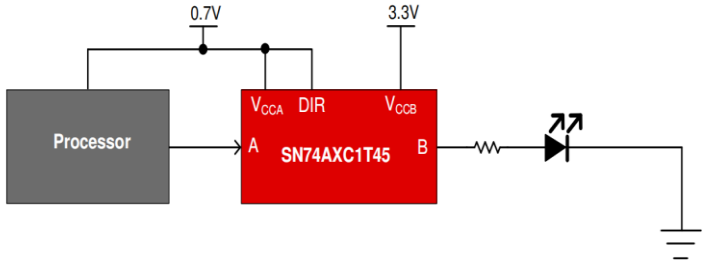
Family	AXC	AVC	LVC	LSF	TXB	TXS	AUP	LV1T
Class	Direction controlled			Auto directional			Uni-directional	
Interfaces supported	Push-pull			Open-drain or push-pull	Push-pull	Open-drain	Push-pull	
V_{cc} (V)	0.65 to 3.6	1.2 to 3.6	1.65 to 5.5	0.9 to 5.5	1.2 to 5.5	1.2 to 5.5	0.9 to 3.6	1.65 to 5.5
Drive strength (mA)	12	12	32	—	0.02	0.02	4	8
Max data rate (Mbps)	380	340	300	200	140	100	380	100
Max bits	8	32	16	8	8	8	1	1

Select by interface					
Interface	2 Ch	4 Ch	6 Ch	8 Ch	16 Ch
SPI	—	SN74AXC4T774 TXB0104	—	SN74AXC8T245	SN74AVC16T245
UART	—	SN74AXC4T774 TXB0104	—	SN74AVC8T245 SN74AXC8T245	SN74AVC16T245
JTAG	—	SN74AXC4T774 TXB0104	—	SN74AXC8T245	SN74AVC16T245
I²S	—	TXB0104 SN74AXC4T245	—	SN74AXC8T245	SN74AVC16T245
I²C	TXS0102 LSF0102	TXS0104E LSF0204	—	TXS0108E LSF0108	—
MDIO	TXS0102 LSF0102	TXS0104E LSF0204	—	TXS0108E LSF0108	—
SMBus	TXS0102 LSF0102	TXS0104E LSF0204	—	TXS0108E LSF0108	—
RMII/RGMII	—	—	TXB0106	SN74AXC8T245	SN74AVC16T245
Quad-SPI	—	—	TXB0106	—	—
SDIO	—	LSF0204	—	LSF0108	—

方向控制型电平转换

DIR方向控制拓扑

- VCCA和VCCB两边电平所能支持的大小
- DIR电平决定转换方向



注意点：

(1)DIR为高时，参考电平是VCCA；

(2)电平芯片所能支持的速率；

(3)VCCA和VCCB相对大小要求

The DIR pin determines the direction of signal propagation. With the DIR pin configured HIGH, translation is from Port A to Port B. With DIR configured LOW, translation is from Port B to Port A. The DIR pin is referenced to V_{CCA}, meaning that its logic-high and logic-low thresholds track with V_{CCA}.

Table 7-1. Function Table

INPUT(1) DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

方向控制型电平转换

DIR方向控制注意事项

NOTES:

1. V_{CCI} is the V_{CC} associated with the input port.
2. V_{CCO} is the V_{CC} associated with the output port.
3. V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 5.5V.

BCT0104

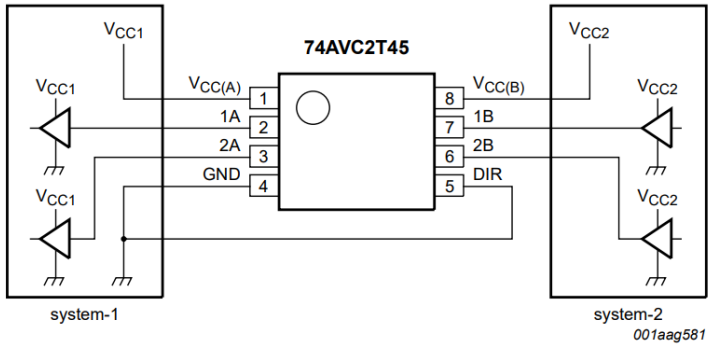
- Wide supply voltage range:
  - $V_{CC(A)}$: 0.8 V to 3.6 V
  - $V_{CC(B)}$: 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- Maximum data rates:
  - 500 Mbit/s (1.8 V to 3.3 V translation)
  - 320 Mbit/s (<1.8 V to 3.3 V translation)
  - 320 Mbit/s (translate to 2.5 V or 1.8 V)
  - 280 Mbit/s (translate to 1.5 V)
  - 240 Mbit/s (translate to 1.2 V)
- Suspend mode
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3B exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

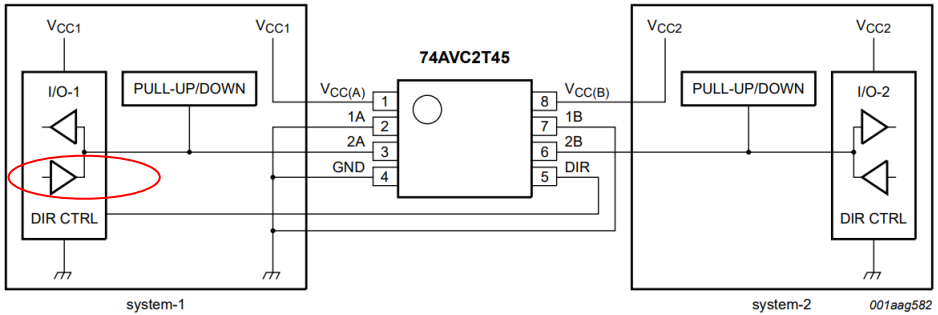
74AVC2T45

方向控制型电平转换

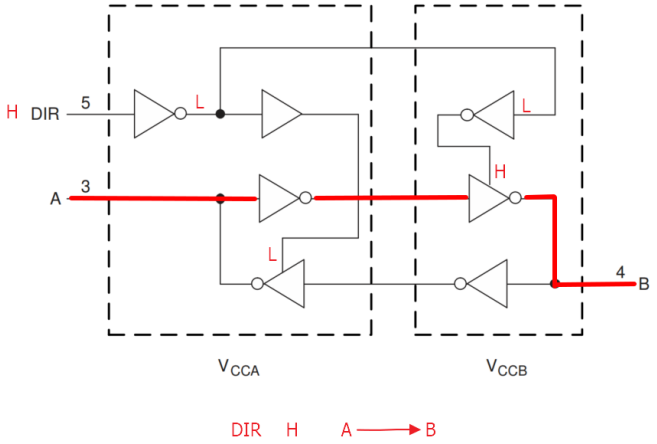
DIR方向控制工作原理

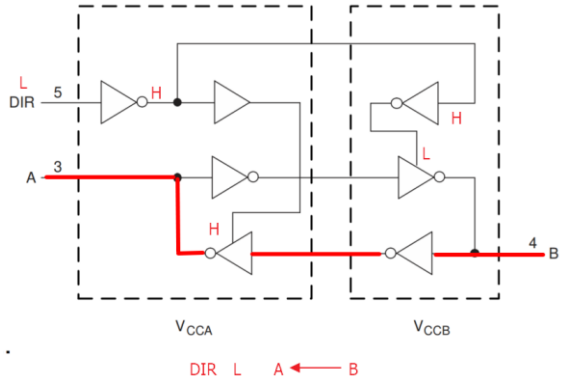
通过控制内部发送器和接收器的开通和关断来实现电平单向传输





System-1 and system-2 must use the same conditions, i.e., both pull-up or both pull-down.

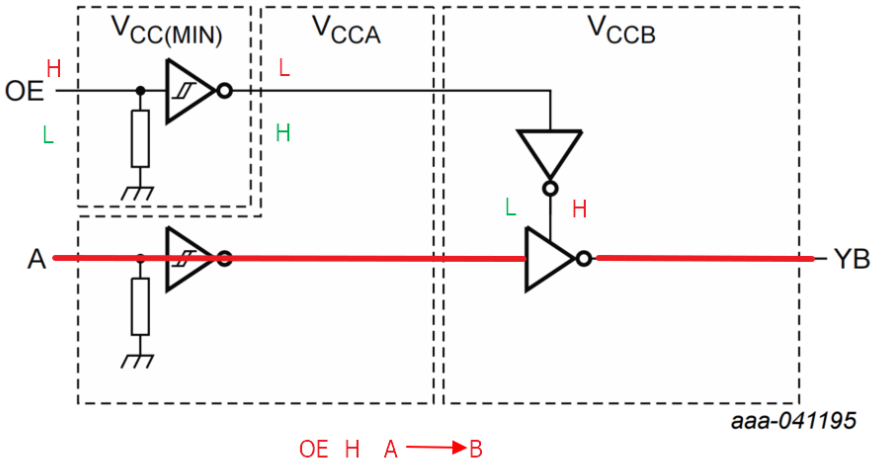




固定方向电平转换

固定方向拓扑

- OE管脚决定信号链路通断
- 信号只能单方向传输



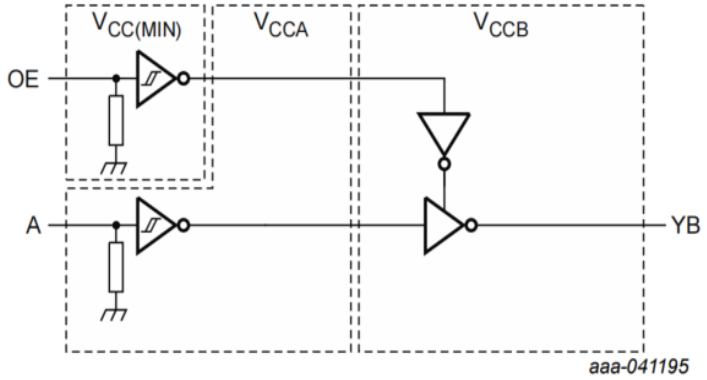


Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

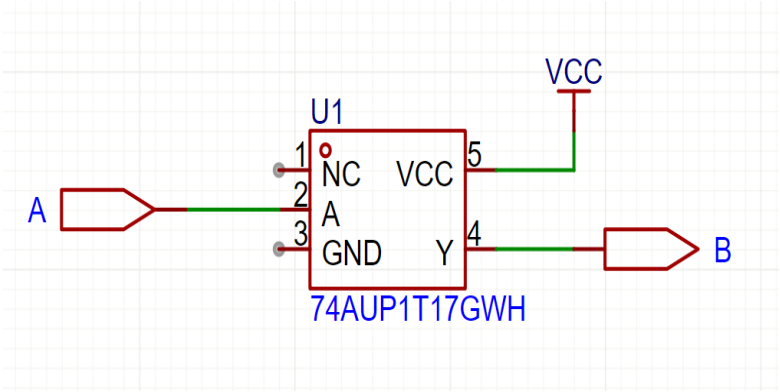
Supply voltage	Input	Input	Output
V_{CCA}, V_{CCB}	OE	A	YB
0.9 V to 5.5 V	H	L	L
0.9 V to 5.5 V	H	H	H
0.9 V to 5.5 V	L	X	Z
GND [1]	X	X	Z
Floating [2]	X	X	Z

NXU0101

固定方向电平转换

固定方向拓扑

- Y端电平由VCCY决定
- 信号传输方向固定



5. Functional diagram

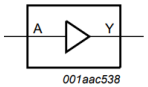


Fig. 1. Logic symbol

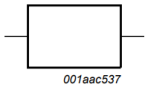


Fig. 2. IEC logic symbol

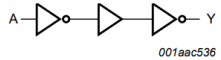


Fig. 3. Logic diagram

74AUP1T34

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
A	**Y**
L	L
H	H

The 74AUP1T34 is a single dual supply translating buffer. Input A is referenced to $V_{CC(A)}$ and output Y is referenced to $V_{CC(Y)}$. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 1.1 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

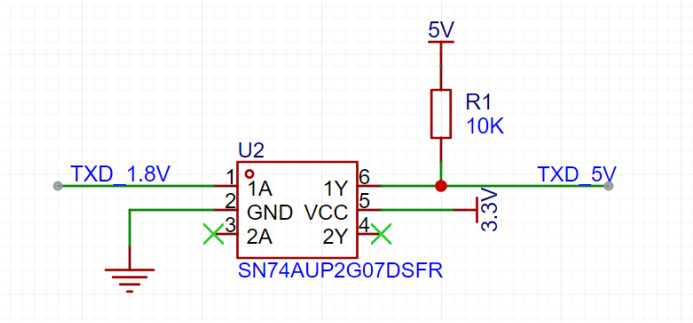
固定方向电平转换

固定方向拓扑

- OD门
- 信号电平由外部上拉电阻决定

注意点：

上拉电阻影响信号速率



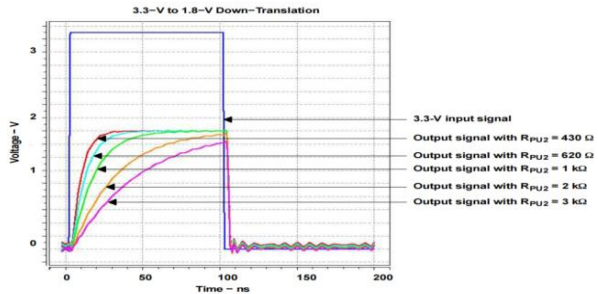


图 7. 通过增加 R_{PU} 的值使输出信号的边沿速率变慢

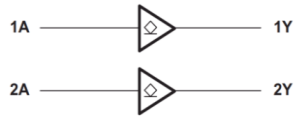
8 Detailed Description

8.1 Overview

The SN74AUP2G07 device is a dual buffer gate with open-drain outputs that operate from 0.8 V to 3.6 V. The output of this dual buffer/driver is open-drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.The I_{off} feature also allows for live insertion.

8.2 Functional Block Diagram



SN74AUP2G07

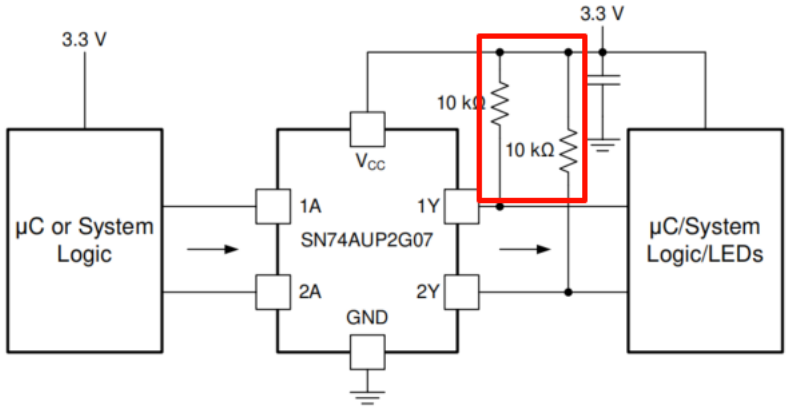


图 9-1. Typical Application Schematic

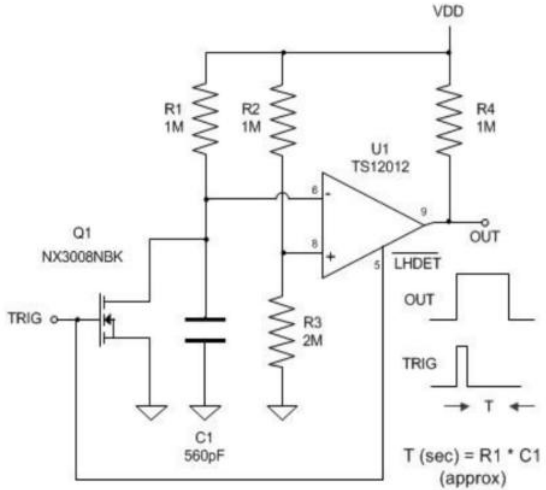
自动识别型电平转换

TXB/NXB型拓扑

➢ 工作原理：

（1）One-shot电路先工作，快速拉高或者拉低

（2） One-shot电路关闭，4KΩ的电阻上拉



D. Ratiometric one-shot (non-inverting)

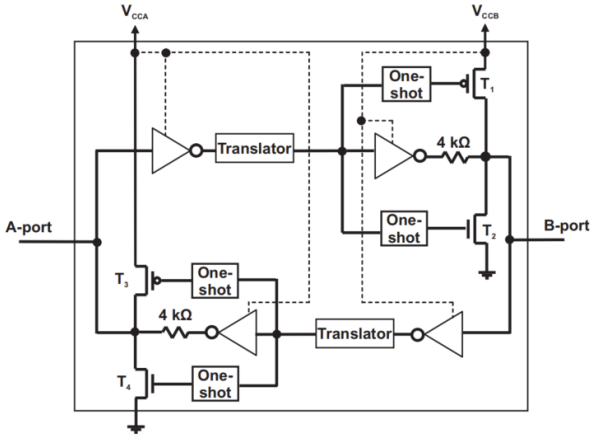
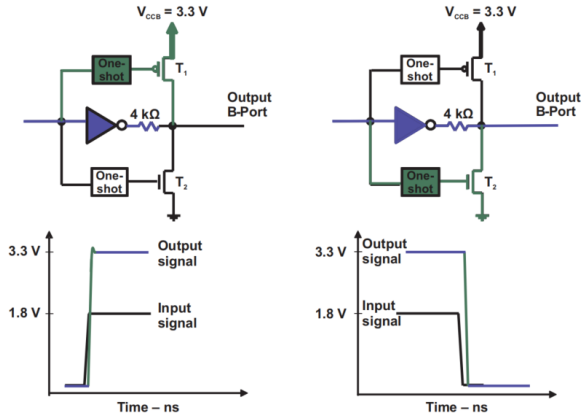


Figure 2. Basic TXB010x Architecture



自动识别型电平转换

TXB/NXB型拓扑外部上下拉

注意点1：上拉电阻影响信号电平

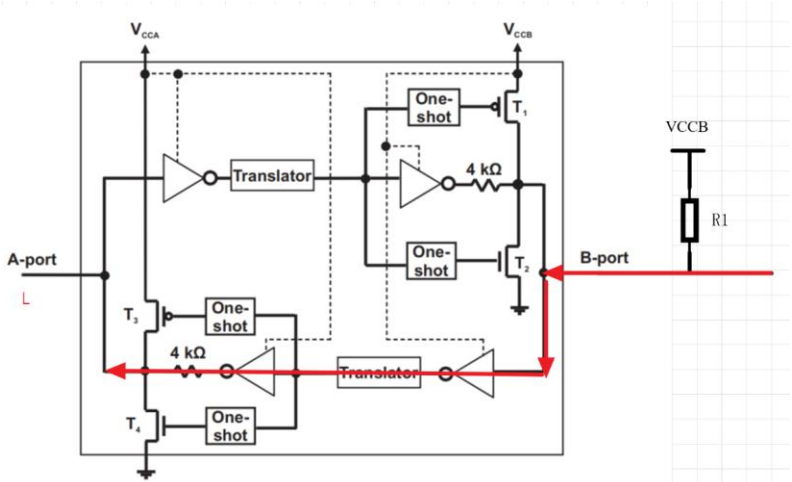


Figure 2. Basic TXB010x Architecture

$$V_{OL} = \frac{4k\Omega}{4k\Omega + R1} \cdot V_{CCB} = \frac{4k\Omega}{4k\Omega + 50k\Omega} \cdot V_{CCB} = 0.075 \cdot V_{CCB}$$

12.7. Pull-up or pull-down resistors on I/O lines

As mentioned previously the NXB0104-Q100 is designed with low static drive strength to drive capacitive loads of up to 70 pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50 kΩ. For this reason the NXB0104-Q100 is not recommended for use in open drain driver applications such as 1-Wire or I^2C. For these applications, the NXS0104-Q100 level translator is recommended.

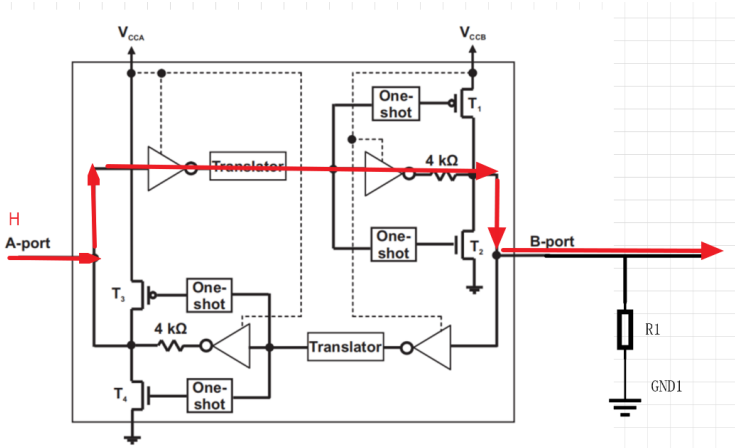


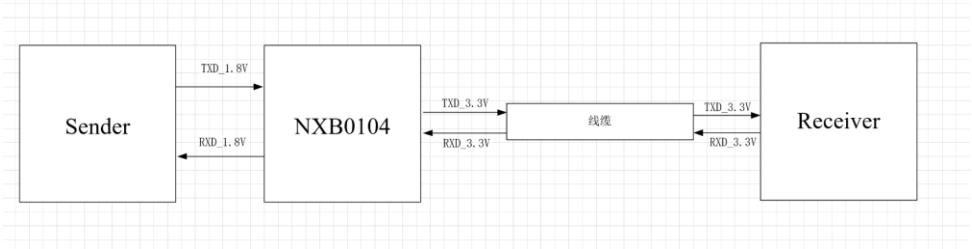
Figure 2. Basic TXB010x Architecture

$$V_{OH} = \frac{R1}{4k\Omega + R1} \cdot V_{CCB} = \frac{50k\Omega}{4k\Omega + 50k\Omega} \cdot V_{CCB} = 0.925 \cdot V_{CCB}$$

自动识别型电平转换

TXB/NXB型外部负载电容

注意点2：容性负载对信号影线



以需要 1.2V 至 1.8V 转换并以 32Mbps 速率运行的用例为例。如果使用 20+ 电缆探测器件的输出，则可以看到类似于图 4-1 的行为。

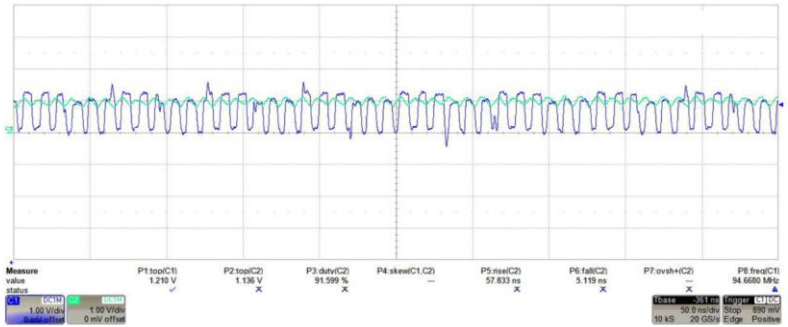


图 4-1. TXB0304，1.2V 至 1.8V 转换，使用二十几英寸输出布线

12.7. Pull-up or pull-down resistors on I/O lines

As mentioned previously the NXB0104-Q100 is designed with low static drive strength to drive capacitive loads of up to 70 pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50 kΩ. For this reason the NXB0104-Q100 is not recommended for use in open drain driver applications such as 1-Wire or I^2C. For these applications, the NXS0104-Q100 level translator is recommended.

NXB0104

With regard to capacitive loads, TXB translators are designed to drive up to 70 pF without issue. If capacitive loading is larger than 70 pF, the O.S. will time-out after 10 ns and subsequently turn off before the output voltage is driven fully high or low. From there, the output will continue to rise or fall based on the RC time constant determined by the 4-kΩ buffer, load resistance and capacitive loading. To ensure reliable operation, system designers should keep capacitive loading for the TXB-type devices to 70 pF or less. With no external loading, the one-shot circuits will remain on for approximately 4.5 nsec. The duration of the one-shots is related to the output voltage level. The output high voltage at which O.S. switches off is approximately 95% of full scale, while the output low voltage at which O.S. switches off is approximately 5%.

TXB0104

自动识别型电平转换

TXB/NXB型外部阻抗匹配

注意点3：

（1）外部线缆的长度；

（2）信号链路上串阻对高低电平影线

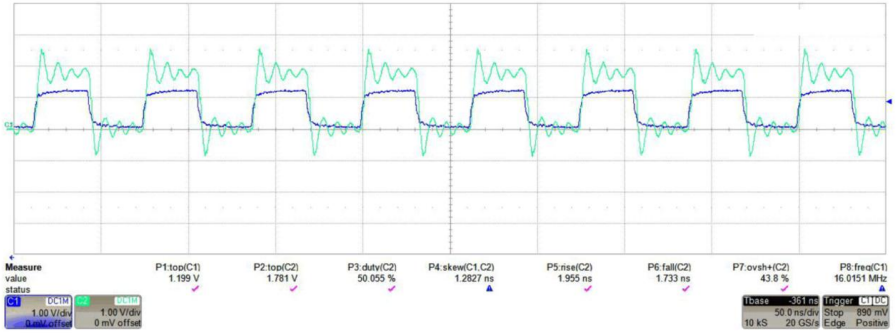


图 4-2. TXB0304，1.2V 至 1.8V 转换，使用 9 英寸输出布线

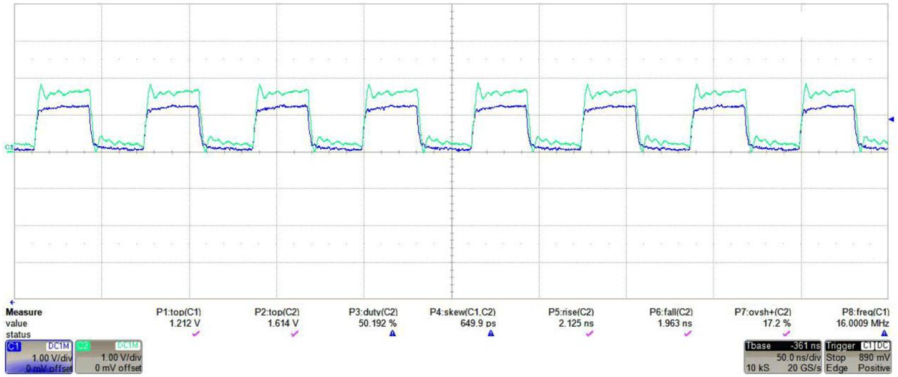


图 4-3. TXB0304，1.2V 至 1.8V 转换，使用 4 英寸输出布线且阻抗与传输线路长度匹配

自动识别型电平转换

TXS/NXS型拓扑

➢ 工作原理：

（1）One-shot电路先工作，快速拉高

（2） One-shot电路关闭，N2 MOS工作

（3）内部10kΩ上拉电阻拉高

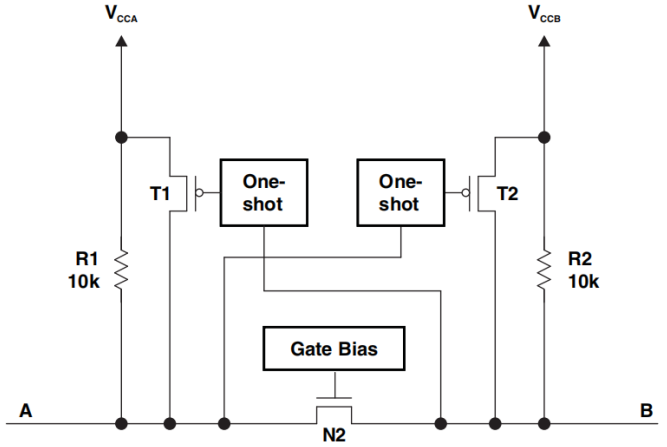
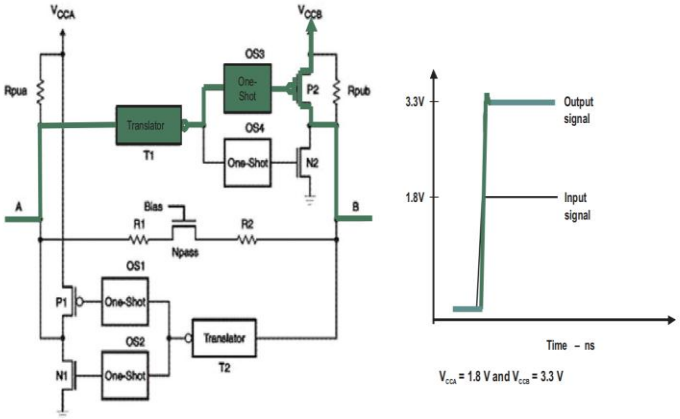
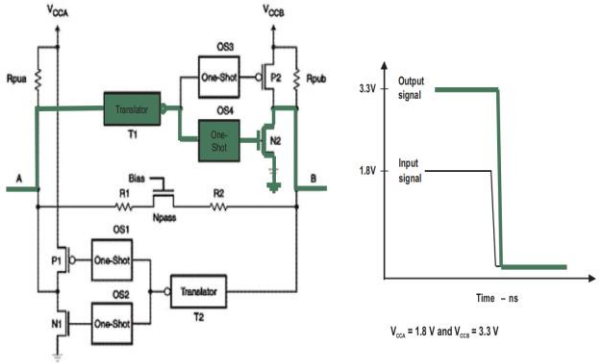


Figure 2. Basic TXS0101, TXS0102, and TXS0104 Architecture

普通型



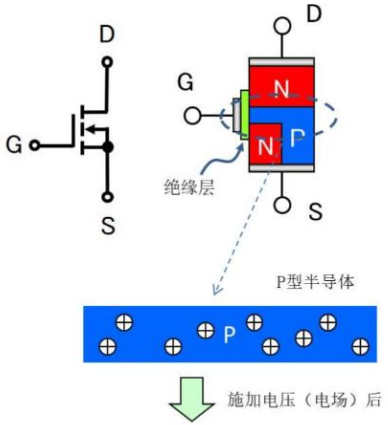
高速型

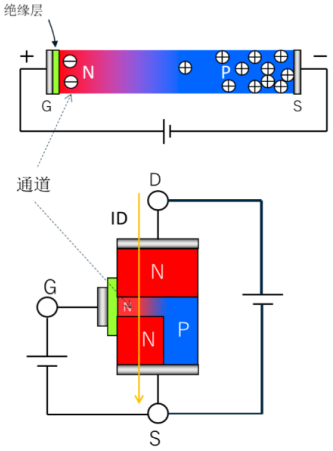


高速型

自动识别型电平转换

TXS/NXS型Pass-gate transistor





These TXS translators are FET-based architectures that utilize an N-channel pass-gate transistor to open and close the connection between the A-port and B-port. When a driver connected to A or B port is low, the opposite port is, in turn, pulled low by the N2 pass-gate transistor. This pass-transistor type voltage translator is ideal for down-translation and over-voltage protection.

Figure 3 shows the transfer characteristics of the N2 pass-gate transistor, where the threshold voltage (V_T) is approximately 1 V and the gate bias voltage (V_{GATE}) is as shown.

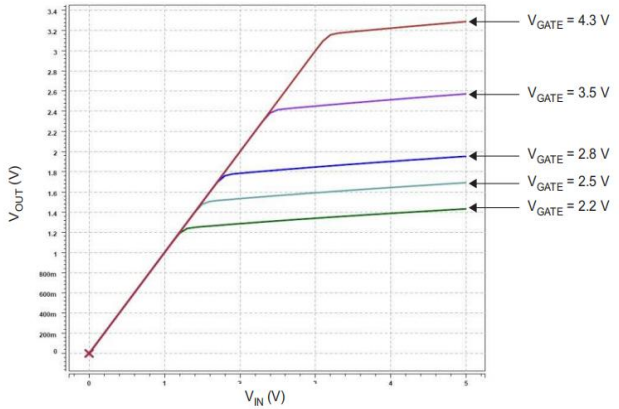
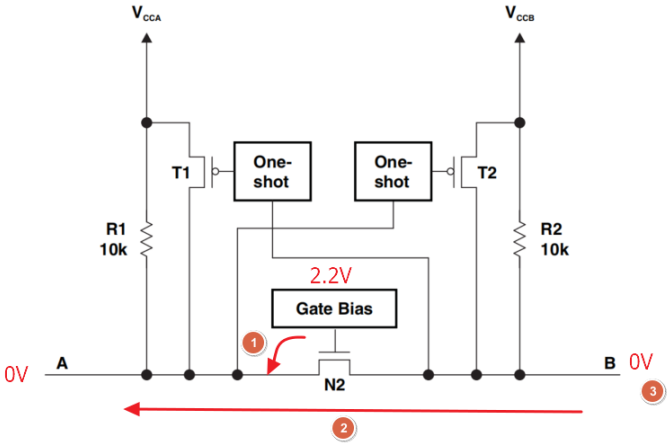
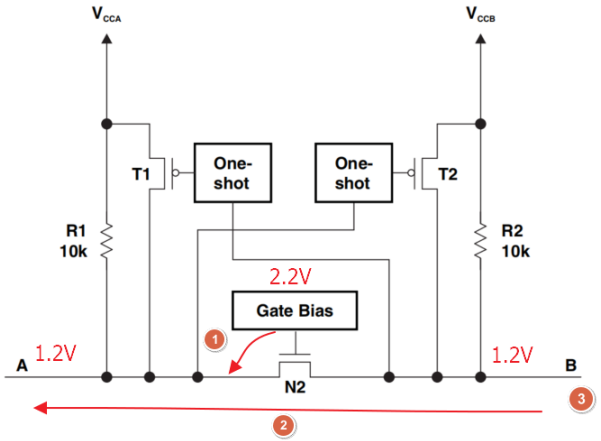


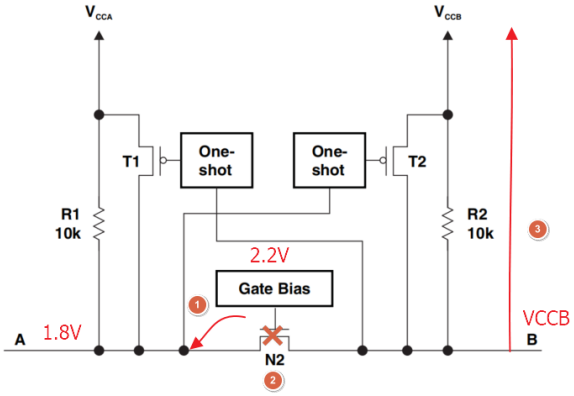
Figure 3. Transfer Characterisitics of an N-Channel Transistor

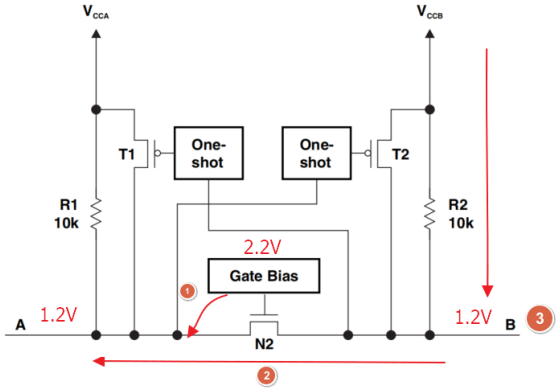
自动识别型电平转换

TXS/NXS型Pass-gate transistor





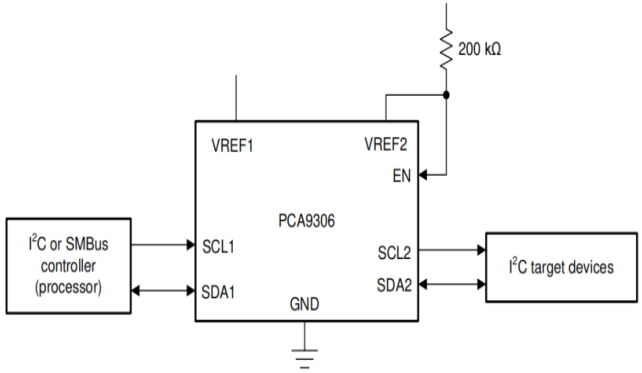


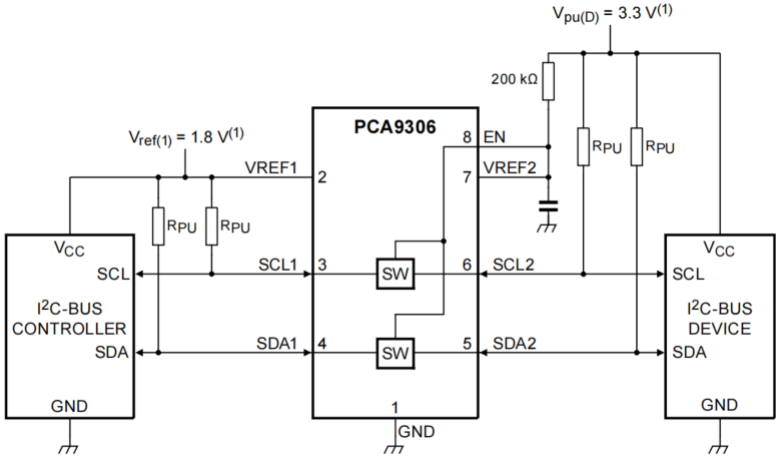


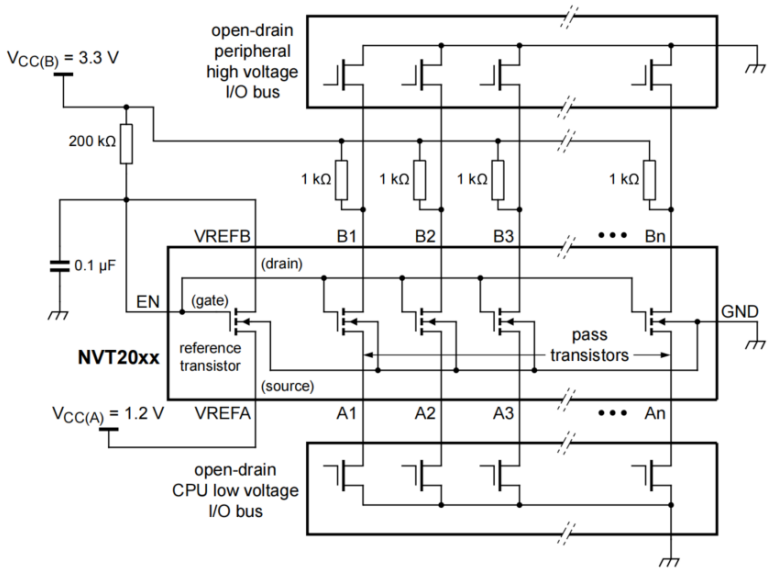
自动识别型电平转换

LSF型拓扑

- 工作原理
- 1个MOS作为参考开关，两端是VREF和EN
- 2个开关的EN连接到参考MOS管



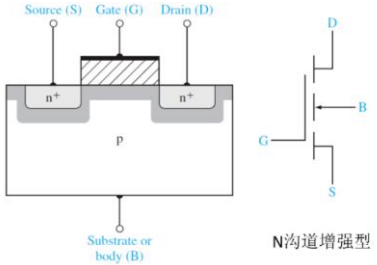




LSF型内部的MOS衬底结GND

自动识别型电平转换

LSF型结构原理



N沟道增强型

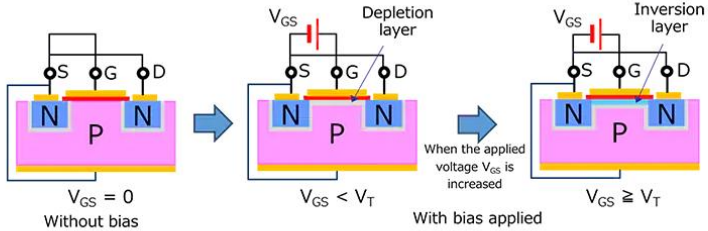
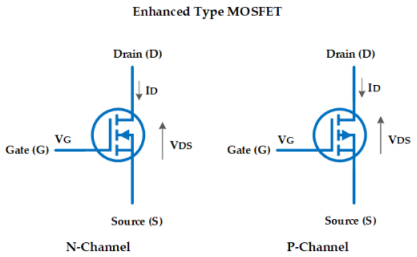
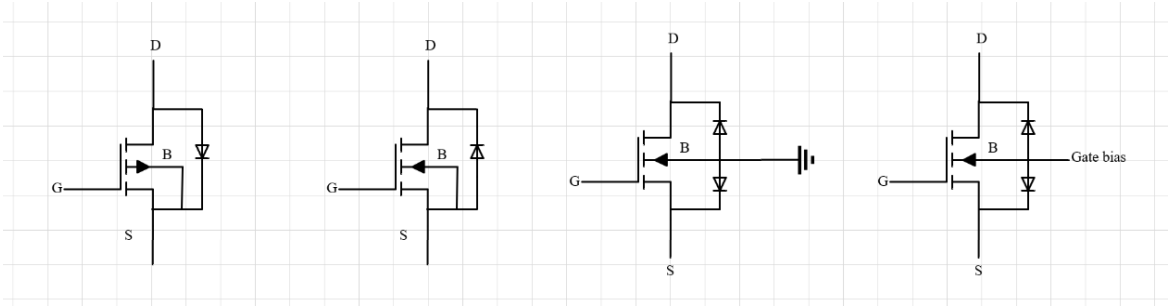


Fig. 7 N-ch MOSFET Formation of inversion layer depending on bias state





1、衬底B和S、D之间会存在PN结,普通MOS的衬底S和B结在一起，在S和D之间形成寄生二极管

2、背靠背的二极管使得MOS管关断时，两边因为二极管背靠背无法传输

3、无论是D还是S端的电压低于Vbias-Vth，MOS均可以导通，实现双向电平转换

自动识别型电平转换

LSF型拓扑内部结构

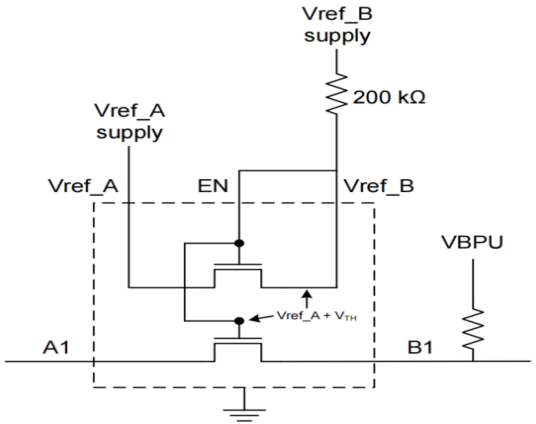


Figure 1. Basics of LSF010x Theory of Operation

内部框图

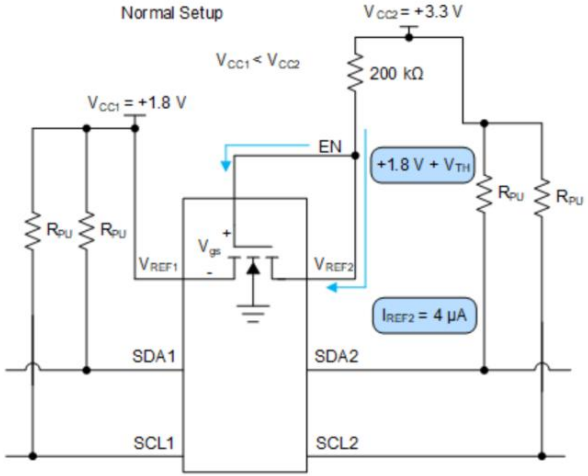


图 8-1. Normal Setup

正确电路

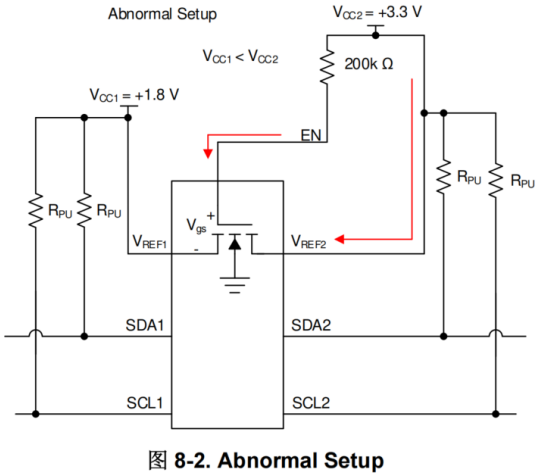


图 8-2. Abnormal Setup

错误电路

1、参考MOS管的EN管脚VEN=VREF1+VTH

2、其他SW（MOS管）的EN管脚和参考管EN连接在一起， VEN1=VREF1+VTH， VEN2=VREF1+VTH

3、当一端的电平小于VREF1时，SW导通，当一端电平等于VREF1，SW临界关断，当一端电平大于VREF1时，SW完全关断

自动识别型电平转换

LSF型拓扑内部结构

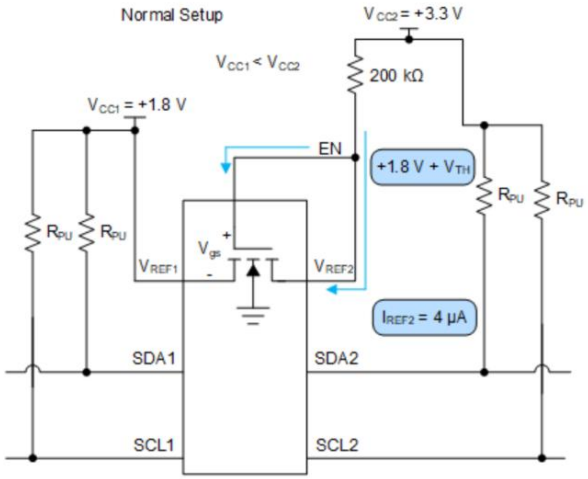


图 8-1. Normal Setup

正确电路

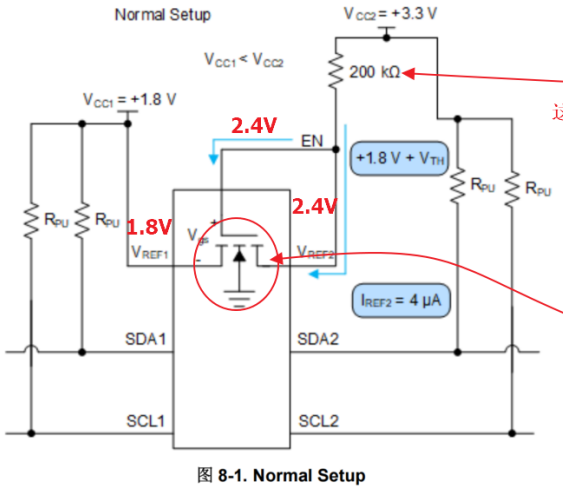


图 8-1. Normal Setup

这个电阻的作用限制**EN**电平

处于临界关断，如果电流要增加，**EN**管脚下降，**MOS**关断，如果电流减小，**EN**管脚增加，**MOS**开通

自动识别型电平转换

LSF型拓扑内部结构

图 8-2 shows an improper set up. If V_{CC2} is larger than V_{CC1} but less than V_{th}, the impedance between V_{CC1} and V_{CC2} is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when V_{CC2} becomes larger than V_{CC1} by V_{th}. During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.

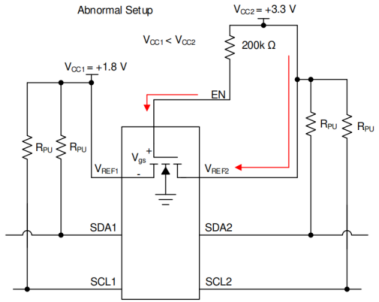
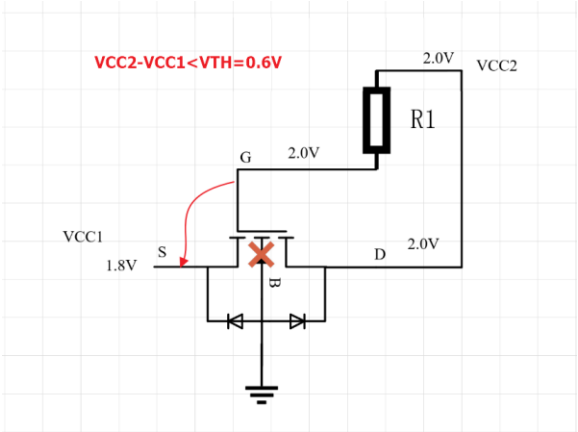
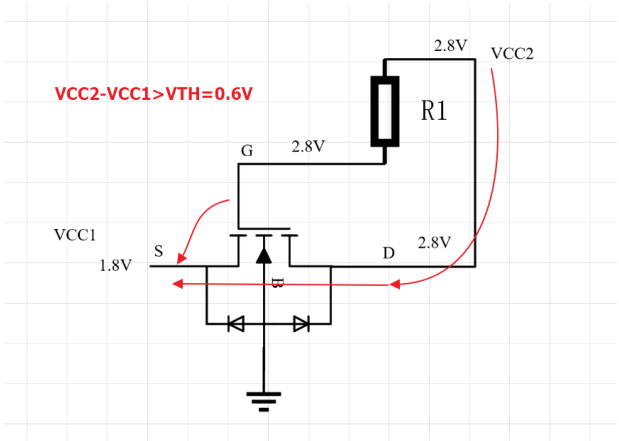


图 8-2. Abnormal Setup

错误电路

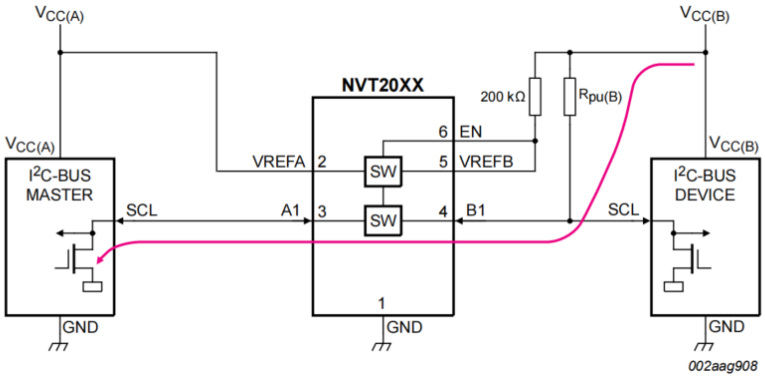




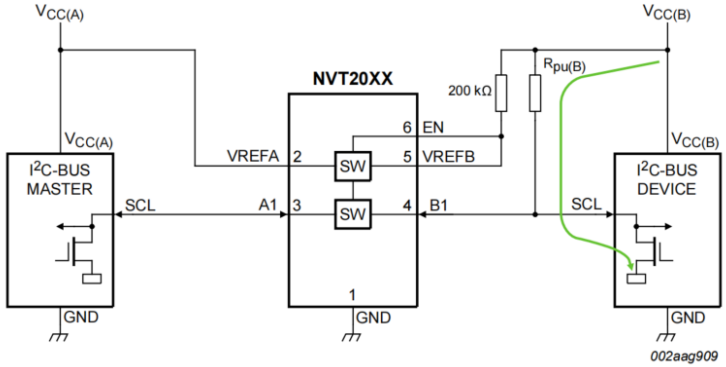
自动识别型电平转换

LSF型拓扑外部上拉电阻

VCC(B) - VCC(A) > 1 V



$$R_{pu(B)} = \frac{V_{CC(B)} - V_{OL(A)}}{I_{D(A)}} - R_{sw} = \frac{3.3V - 0.15V}{10mA} - 3\Omega = 312\Omega$$

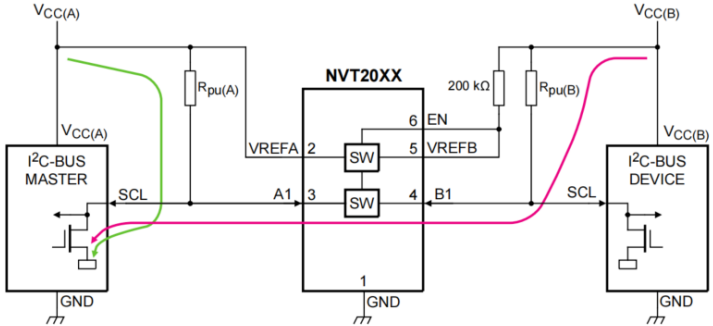


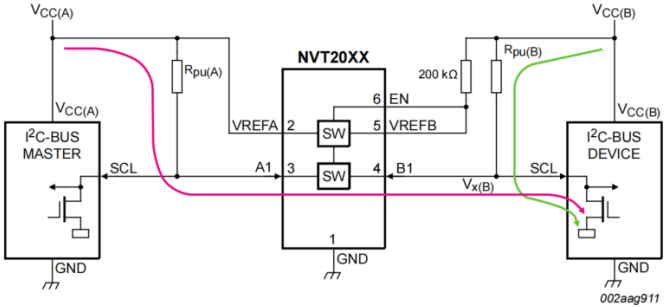
$$R_{pu(B)} = \frac{V_{CC(B)} - V_{IL(A)}}{I_{D(B)}} = \frac{3.3V - 0.15V}{15mA} = 210\Omega$$

自动识别型电平转换

LSF型拓扑外部上拉电阻

VCC(B) - VCC(A) <1 V





$$I_{D(A)} = \frac{V_{CC(A)} - V_{OL(A)}}{R_{pu(A)}} + \frac{V_{CC(B)} - V_{OL(A)}}{R_{pu(B)} + R_{sw}}$$

$$I_{D(B)} = \frac{V_{CC(A)} - V_{IL(A)}}{R_{pu(A)}} + \frac{V_{CC(B)} - V_{x(B)}}{R_{pu(B)}}$$

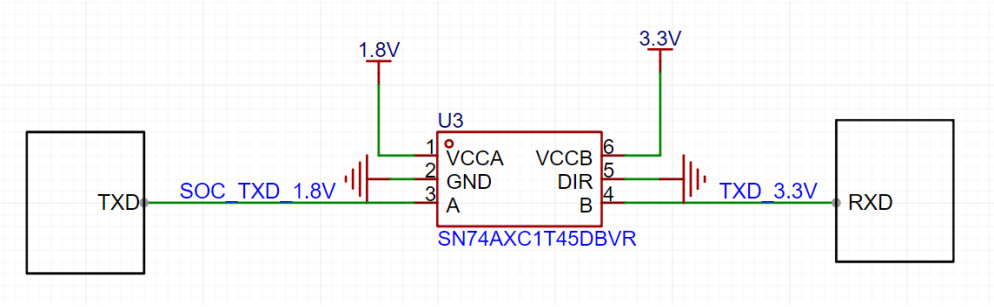
$$V_{x(B)} = V_{CC(A)} - \left(\frac{V_{CC(A)} - V_{IL(A)}}{R_{pu(A)}} \right) \times \left(R_{pu(A)} + R_{sw} \right)$$

$$R_{pu} = \frac{V_{CC(A)} - V_{OL(A)} + V_{CC(B)} - V_{OL(A)}}{I_{D(A)}} = \frac{2.5V - 0.25V + 3.3V - 0.25V}{10mA} = 530\Omega$$

$$R_{pu} = \frac{V_{CC(A)} - V_{IL(A)} + V_{CC(B)} - V_{IL(A)}}{I_{D(B)}} = \frac{2.5V - 0.25V + 3.3V - 0.25V}{15mA} = 353\Omega$$

案例1：UART转换失败

SOC给外设发送信号，DIR配置错误导致TXD通信失败



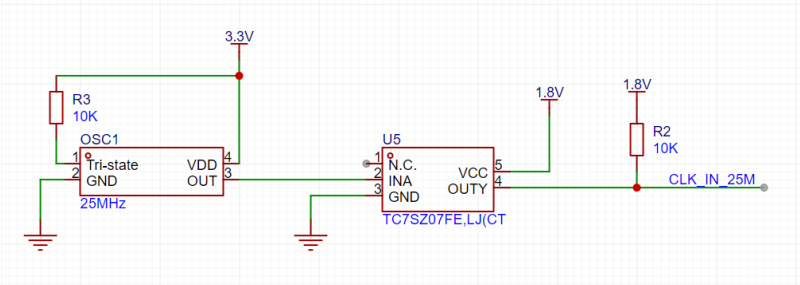
3 说明

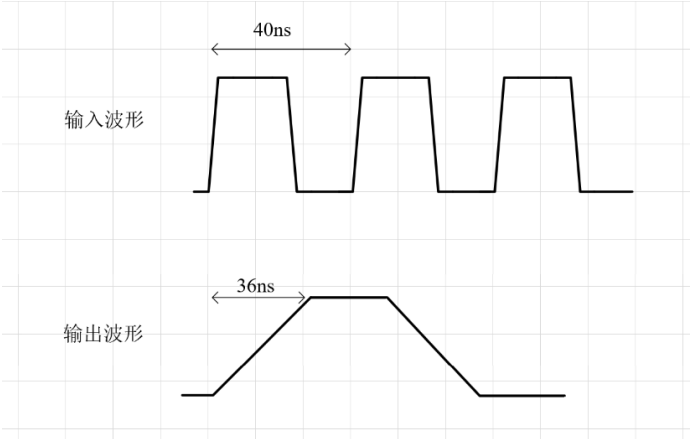
SN74AXC1T45 是一款采用两个独立可配置电源轨的单比特位同相总线收发器。V_{CCA} 和 V_{CCB} 电源电压低至 0.65V 时，该器件可正常工作。A 端口用于跟踪 V_{CCA}，该端口可支持 0.65V 至 3.6V 范围内的任何电源电压。B 端口用于跟踪 V_{CCB}，该端口也可支持 0.65V 至 3.6V 范围内的任何电源电压。

DIR 引脚决定信号传播的方向。DIR 引脚配置为高电平时，信号转换由端口 A 流向端口 B。DIR 配置为低电平时，则由端口 B 流向端口 A。DIR 引脚以 V_{CCA} 为基准，这意味着它的逻辑高电平和逻辑低电平阈值跟踪 V_{CCA} 电压。

案例2：OD门输出时钟非方波

按照最大上升时间计算，20ns/V，从0V上升到1.8V，需要36ns。时钟周期是40ns，无法实现正常的电平转换



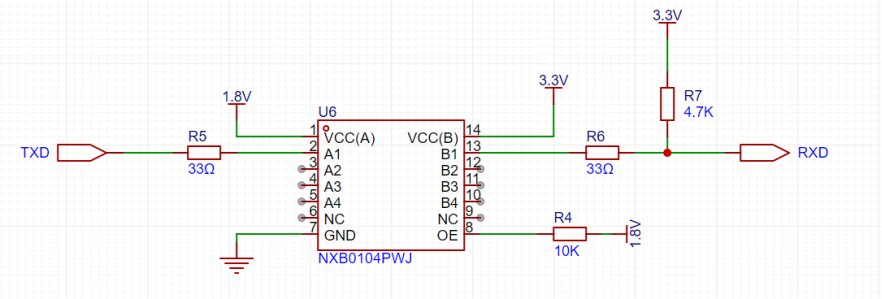


8. Operating Ranges (Note)

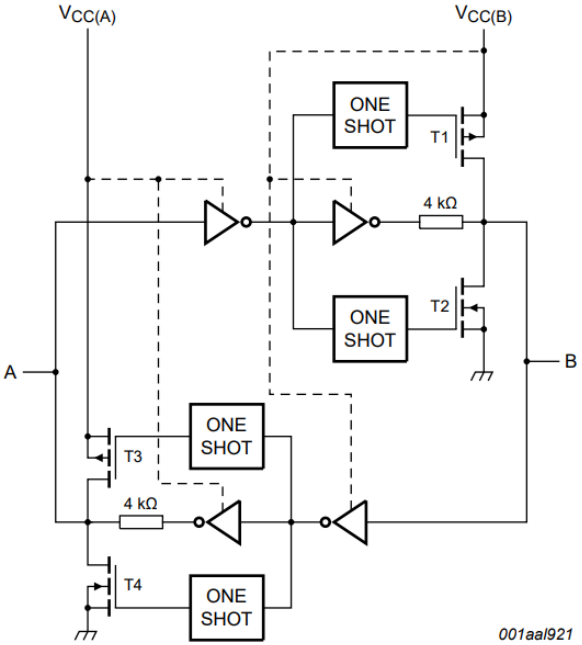
Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CC}		—	1.65 to 5.5	V
		(Note 1)	—	1.5 to 5.5	
Input voltage	V_{IN}		—	0 to 5.5	V
Output voltage	V_{OUT}		—	0 to 5.5	V
Operating temperature	T_{opr}	(Note 2)	—	-40 to 125	°C
		(Note 3)	—	-40 to 85	
Input rise and fall time	dt/dv		V_{CC} = 1.8 ± 0.15 V, 2.5 ± 0.2 V	0 to 20	ns/V
			V_{CC} = 3.3 ± 0.3 V	0 to 10	
			V_{CC} = 5.0 ± 0.5 V	0 to 5	

电平转换案例

案例3：上拉电阻导致低电平抬高



$$V_{OL} = \frac{4k\Omega}{4k\Omega + R7} \cdot V_{CCB} = \frac{4k\Omega}{4k\Omega + 4.7k\Omega} \cdot V_{CCB} = 0.45 \cdot V_{CCB} = 1.52V$$



参考资料

A Guide to Voltage Translation With TXB-Type Translators

A Guide to Voltage Translation With TXS-Type Translators

Voltage-Level Translation With the LSF Family